

Drawing Amendments:

The attached 39 sheets of drawings include changes to FIGs. 1-43 correcting various informalities identified during the prosecution of the related cases. No new matter has been introduced. These sheets replace the original sheets including FIGs. 1-43.

**REPLACEMENT
DRAWING**

App. No. 09/491,121
Inventor: Branko Kovacevic et al.
Attorney: J. Gustav Larson (512 327-5515)



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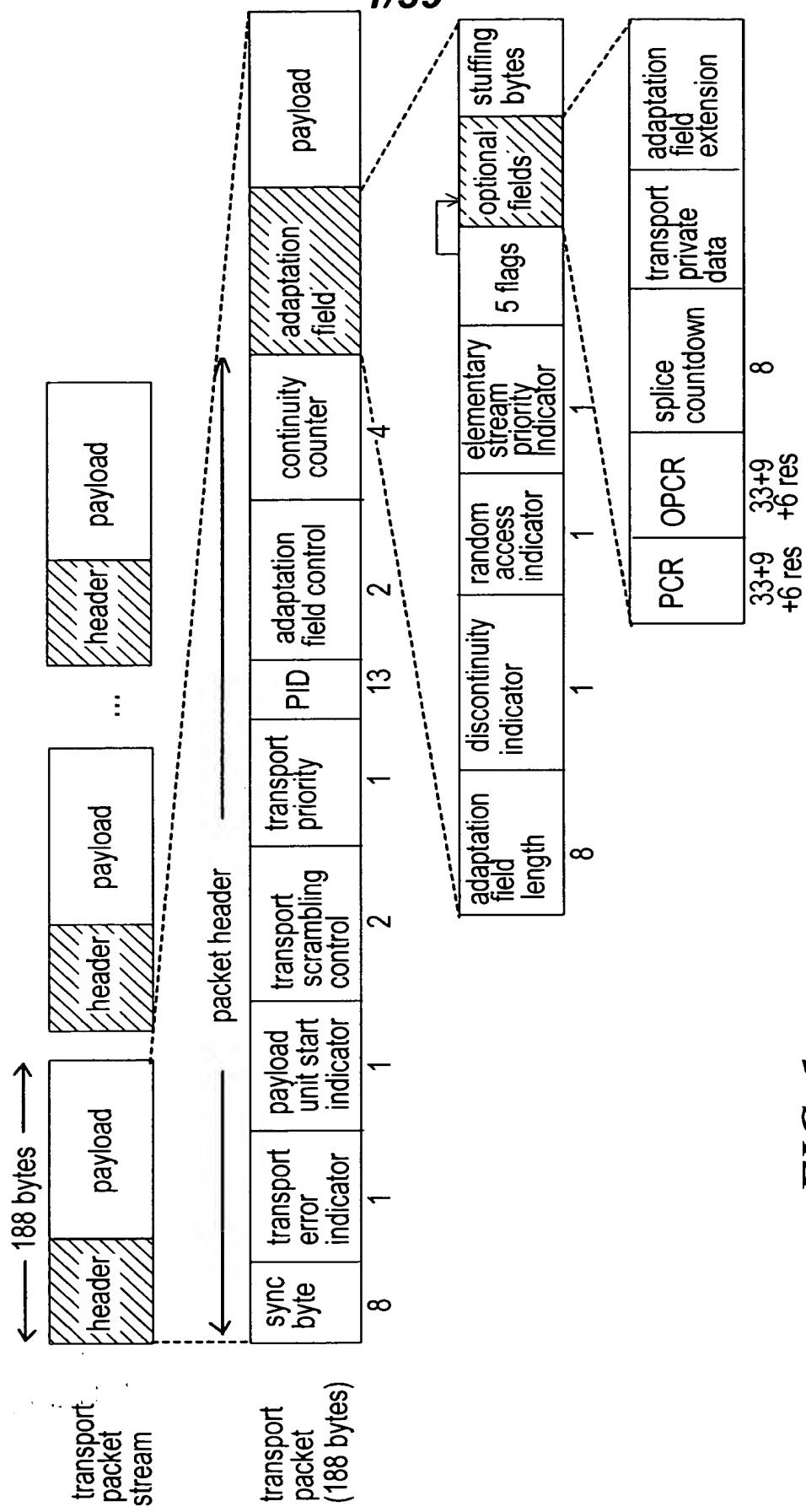


FIG. 1
--PRIOR ART--

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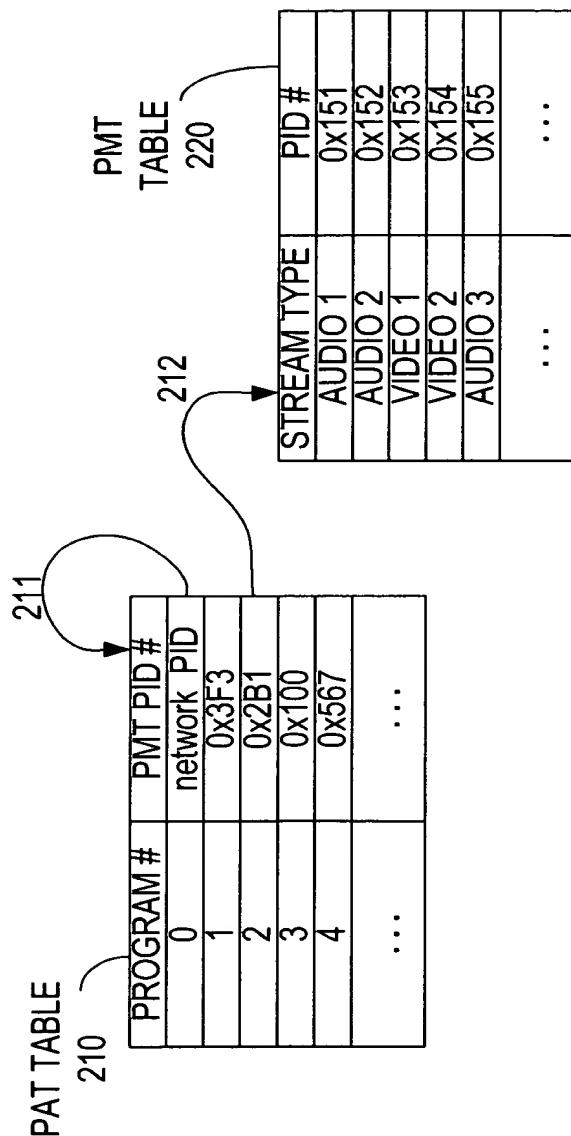


FIG. 2
-PRIOR ART--



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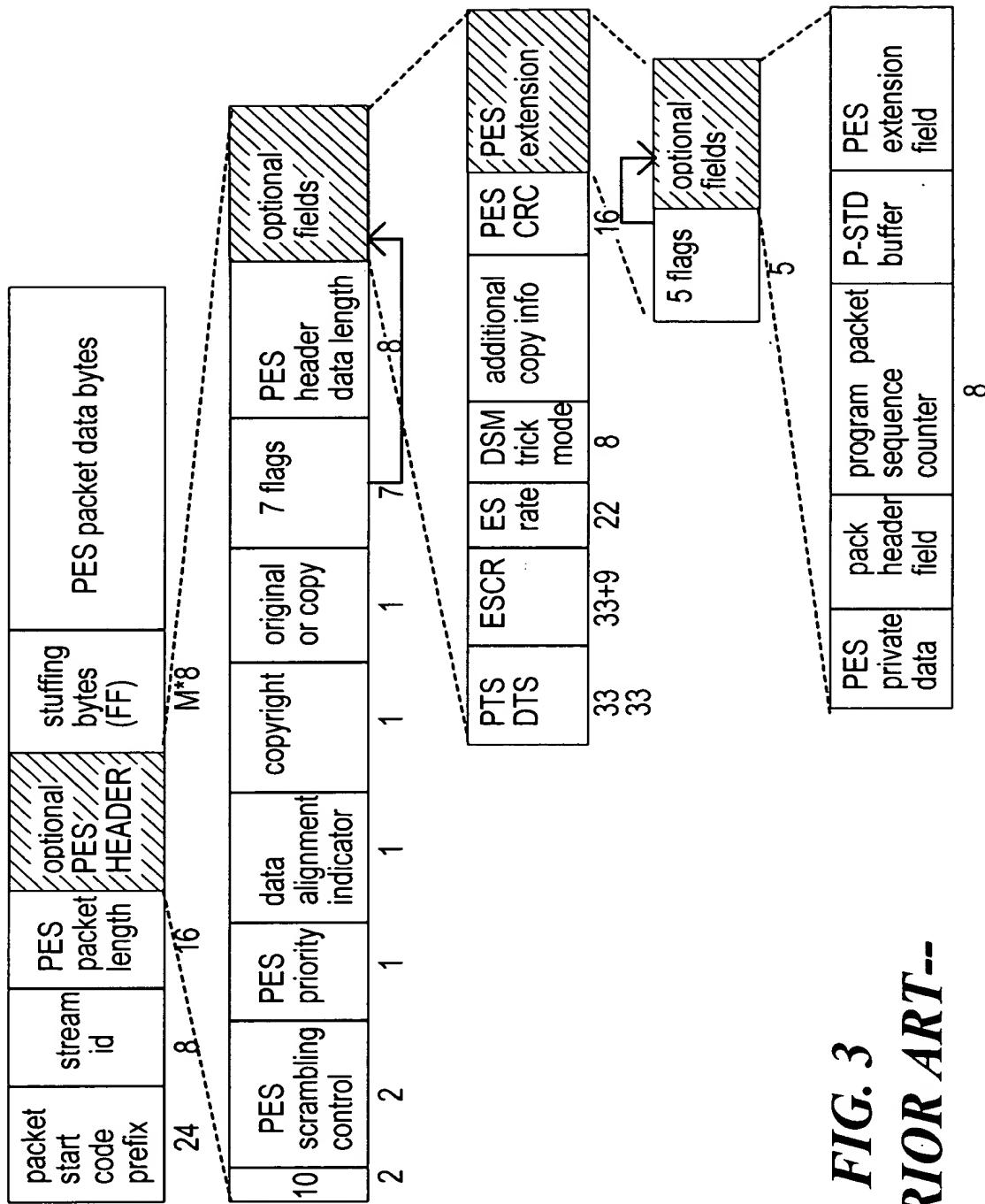


FIG. 3
--PRIOR ART--

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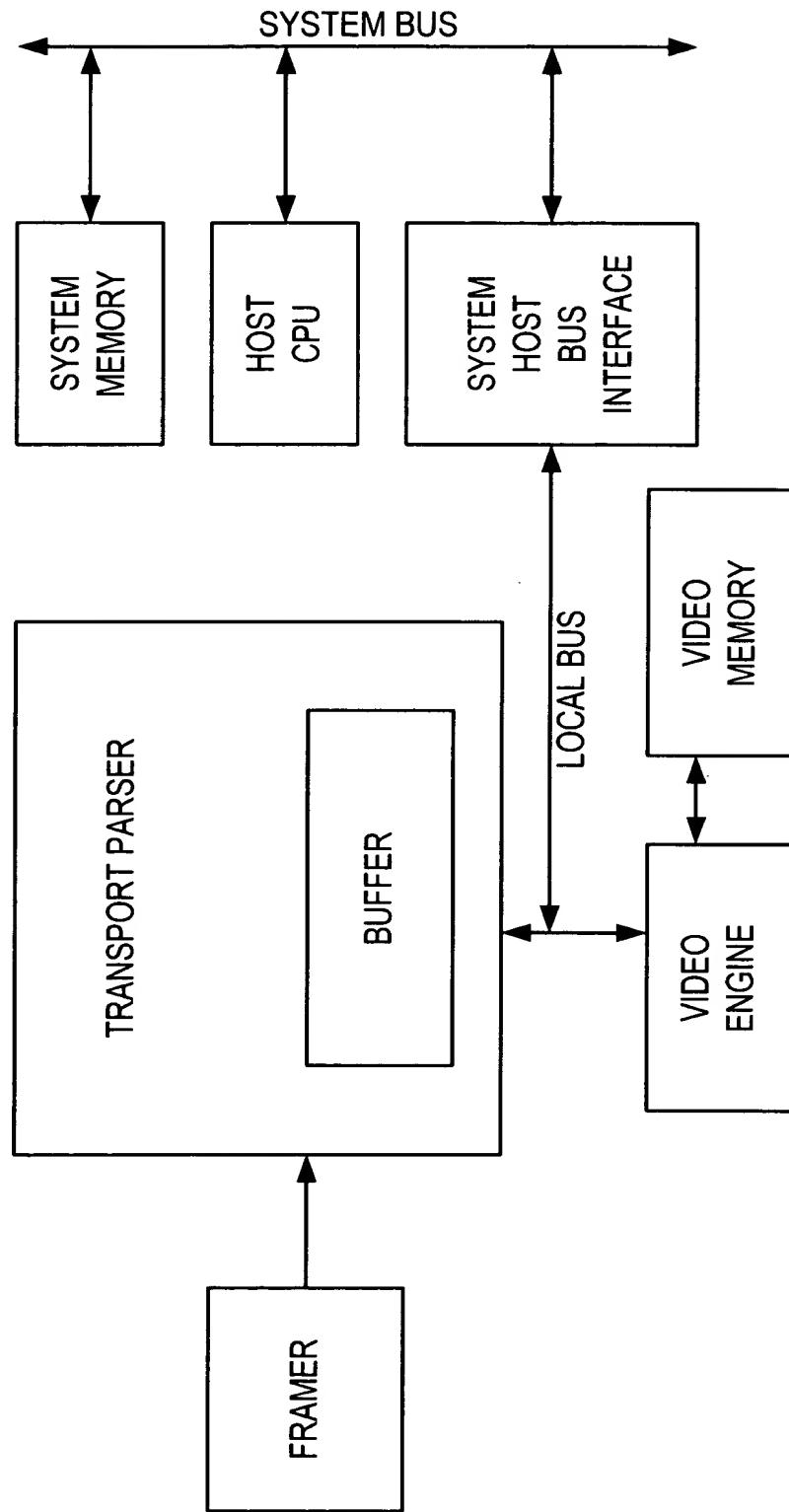


FIG. 4
--PRIOR ART--

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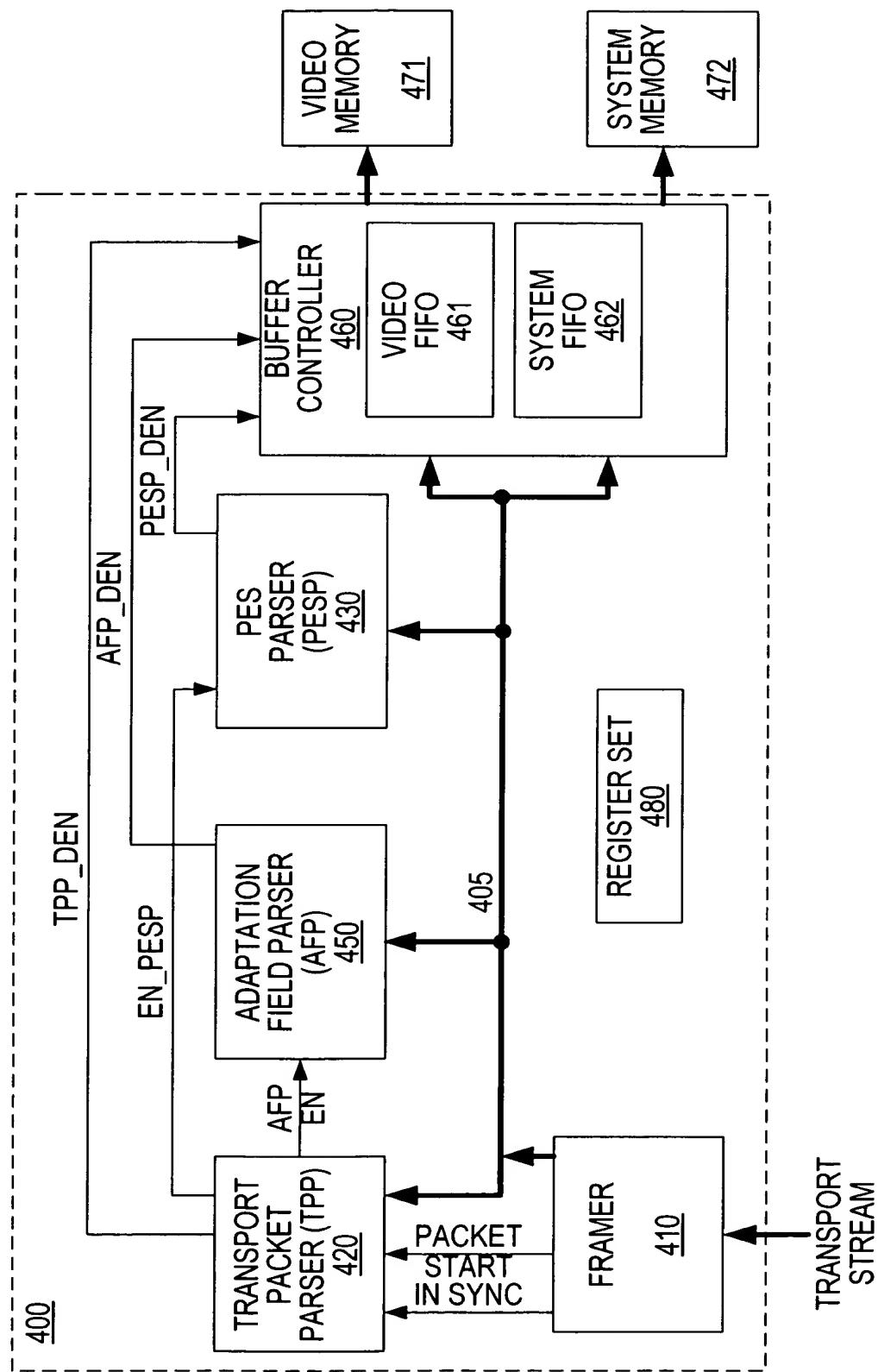
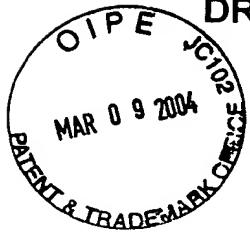


FIG. 5

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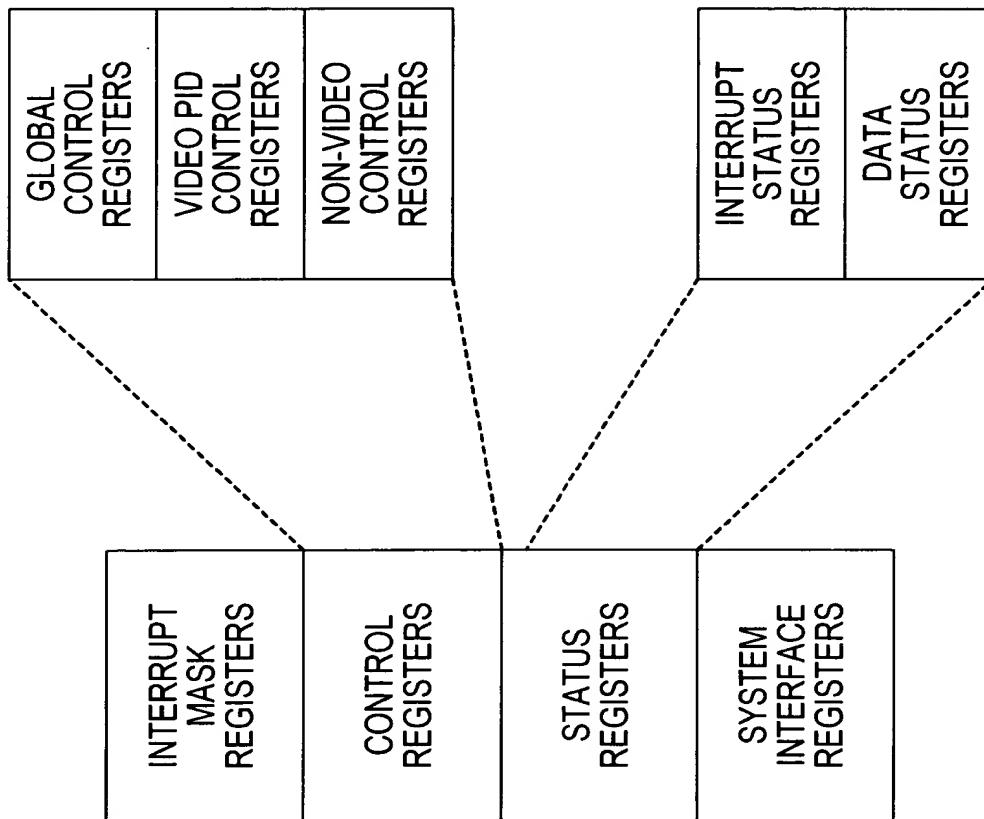


FIG. 6

480

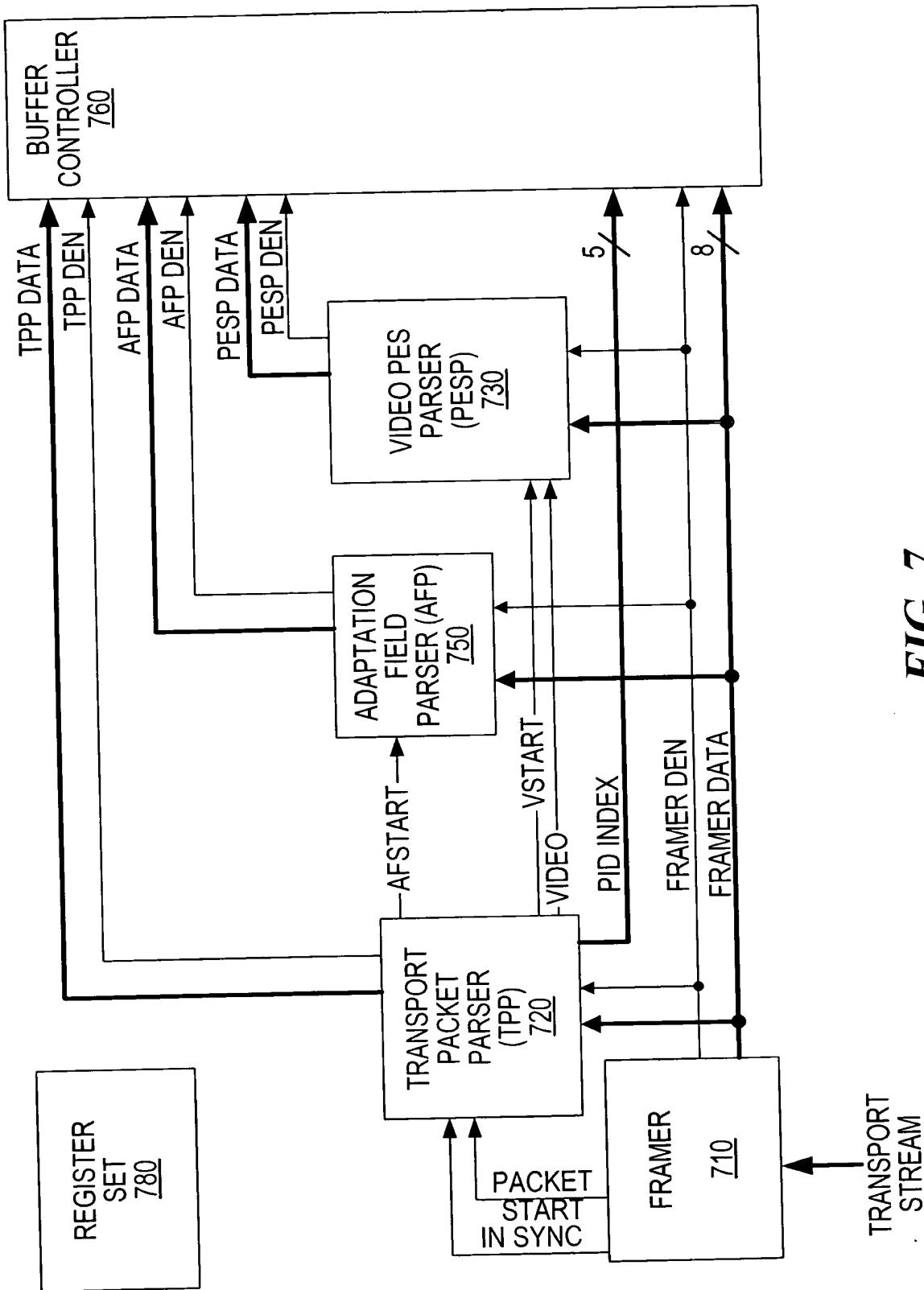


FIG. 7

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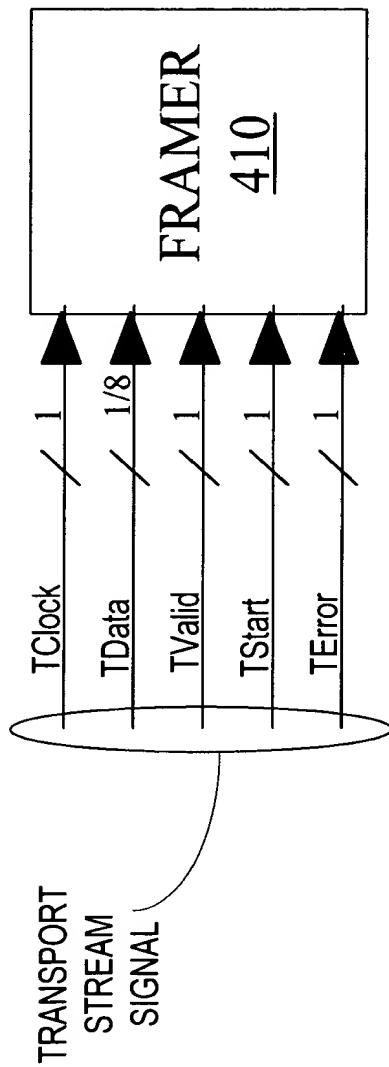


FIG. 8

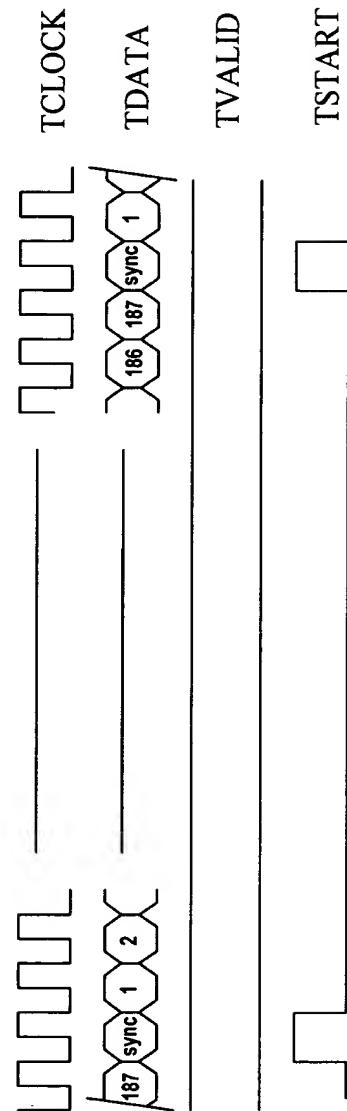


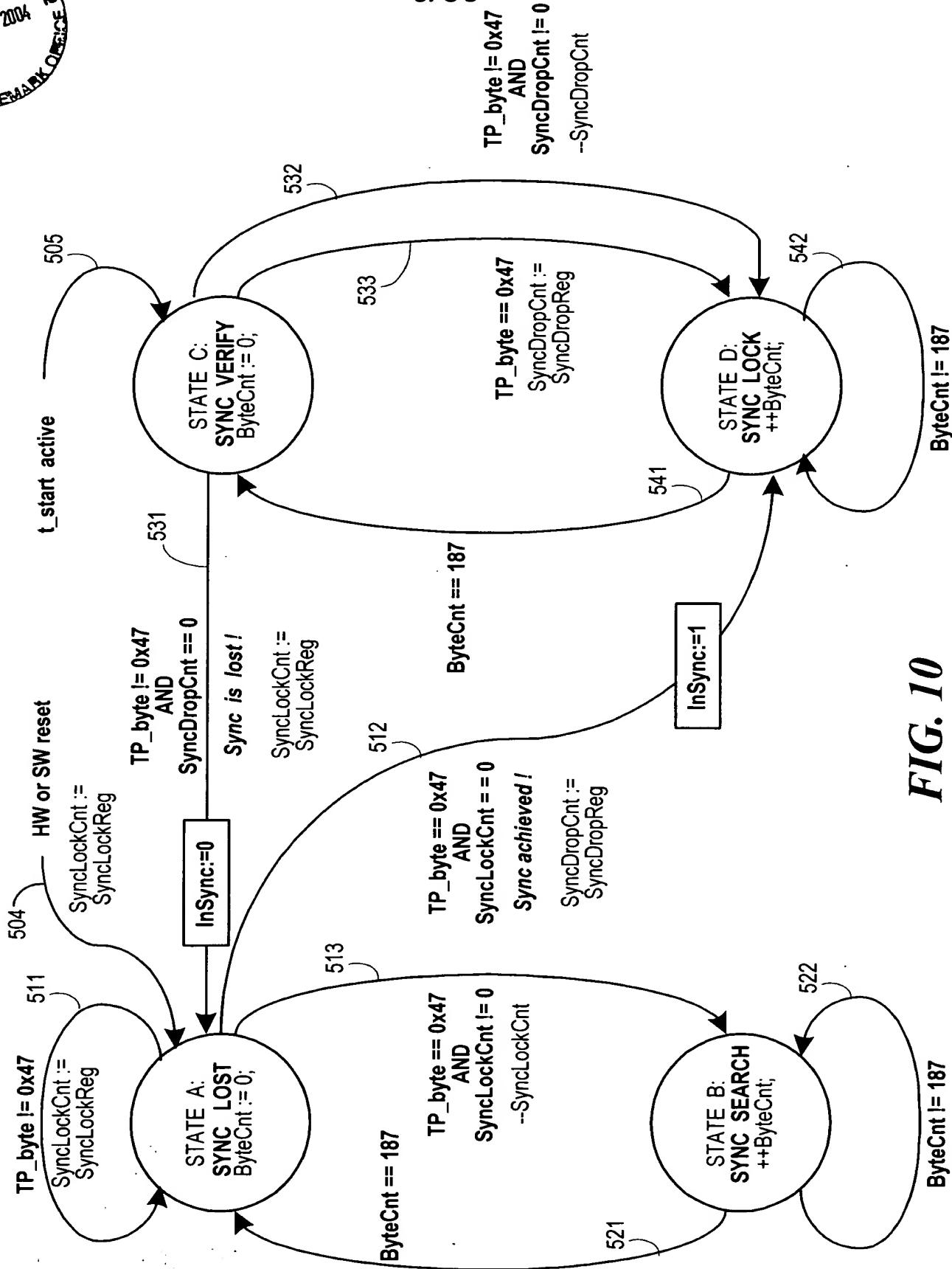
FIG. 9

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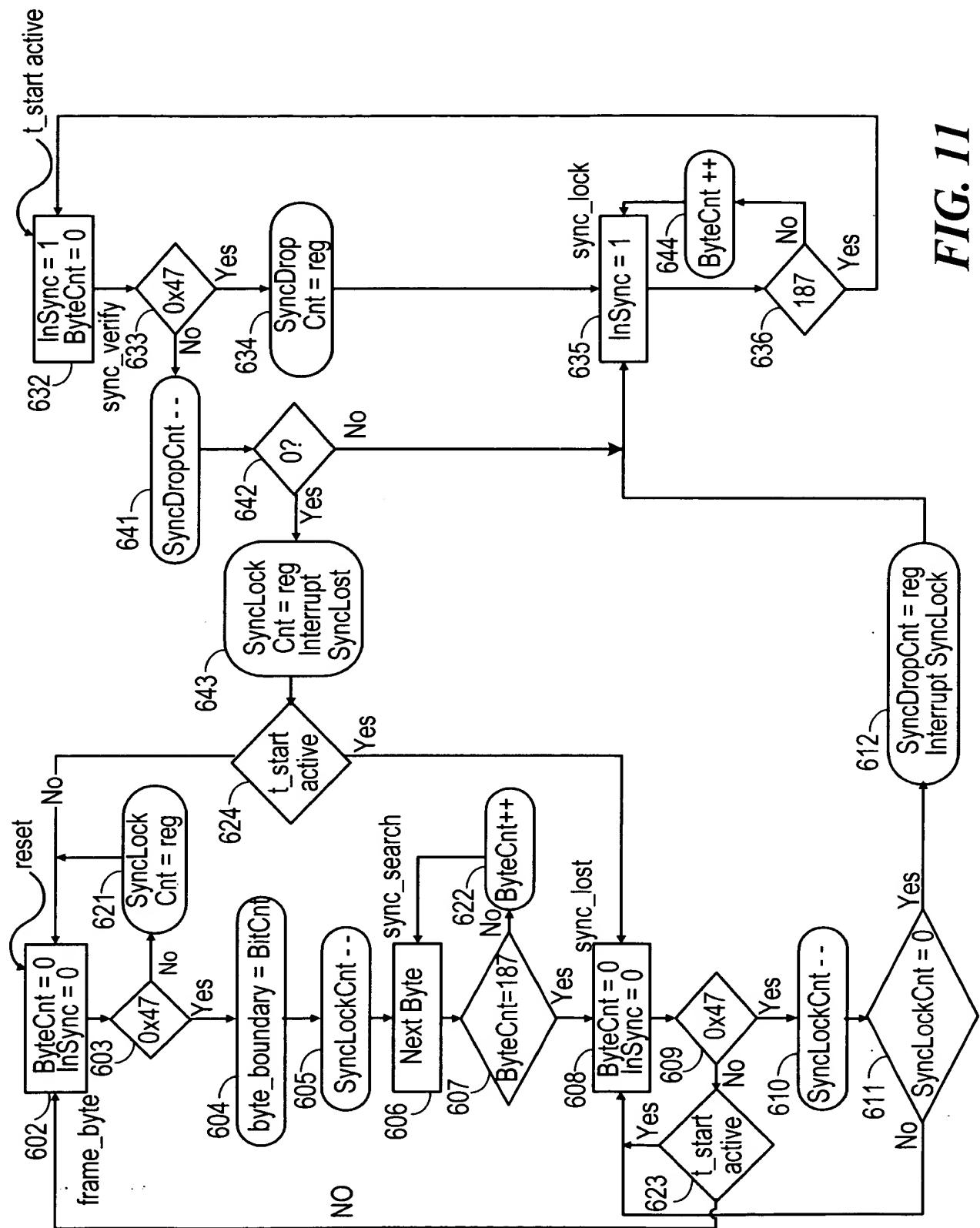


FIG. 11

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Transport Demultiplexer Global Status Register					
Field Name	Bits	Len	Default	Type	Description
FramerSyncLock	0	[1]	0	R/W	This bit is set to '1' after the frame synchronization has been acquired. WR_ACC_CLEAR .
FramerSyncDrop	1	[1]	0	R/W	This bit is set to '1' after the frame synchronization has been lost. WR_ACC_CLEAR .
CurrentFramerState	20-22	[3]	'000'	R	<p>This 3 bit field codes the current state of the framer.</p> <ul style="list-style-type: none"> '000' – Capturing a byte '001' – Out of TP frame synchronization '010' – Searching for synchronization '011' – Checking for synchronization '100' – In the TP frame synchronization <p>NOTE: Only a framer state machine updates this field. Write access does not modify it.</p>
UnusedField	29-31	[3]	'000'	R/W	Unused and reserved field.

FIG. 12

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Transport Demultiplexer Interrupt Mask Register				
Field Name	Bits	Len	Default	Type
EventInterruptMask	0-18 [19]	0	0	R/W
				If set to '1' enables local sources of interrupts.
				Bit 0 – FrameSyncLock Bit 1 – FrameSyncDrop
				Bits 2 – 19 Other Functionality
EnableGlobalDemuxInterrupt	20 [1]	0	0	R/W
UnusedField	21-31 [11]	0	0	R/W
				If set to '1' enables globally TD core interrupts. Unused and reserved field. Always set to 0.

FIG. 13

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Transport Demultiplexer Global Control Register					
Field Name	Bits	Len	Default	Type	Description
FramerSyncLockLength	0-4 [5]	00101	R/W	Five bits field to select a number of consecutive transport packets after MPEG-2 frame (bit-stream) synchronization is declared.	
FramerSyncDropLength	5-7 [3]	011	R/W	Three bits field to select a number of consecutive transport packets after a loss of MPEG -2 frame synchronization is declared.	
FramerBitPolarity	8 [1]	0	R/W	'0' selects msb first (default mode), '1' select lsb first	
FramerClockPolarity	9 [1]	0	R/W	If set to '0' framer will latch on falling edge (default) If set to '1' framer will latch on rising edge.	
FramerMode:	10-11 [2]	'00'	R/W	Defines a combination of external control signals: '00' – Framer uses T_start only. '01' – Framer uses T_valid only. '10' – Framer uses T_start and T_valid. '11' – Framer uses T_clock and T_data only.	
Other Functionality Bits	12-15 [4]			Other functionality (not relevant to Framer)	
T_ValidPolarity	16 [1]	1	R/W	'1' selects active high [5V] for t_valid external signal	
T_StartPolarity	17 [1]	1	R/W	'1' selects active high [5V] for t_start external signal	
T_ErrorPolarity	18 [1]	1	R/W	'1' selects active high [5V] for t_error external signal	
Other Functionality Bits	19-28 [10]			Other functionality (not relevant to Framer)	
UnusedField	29-31 [3]	0	R/W	Unused and reserved field. Always set to 0.	

FIG. 14

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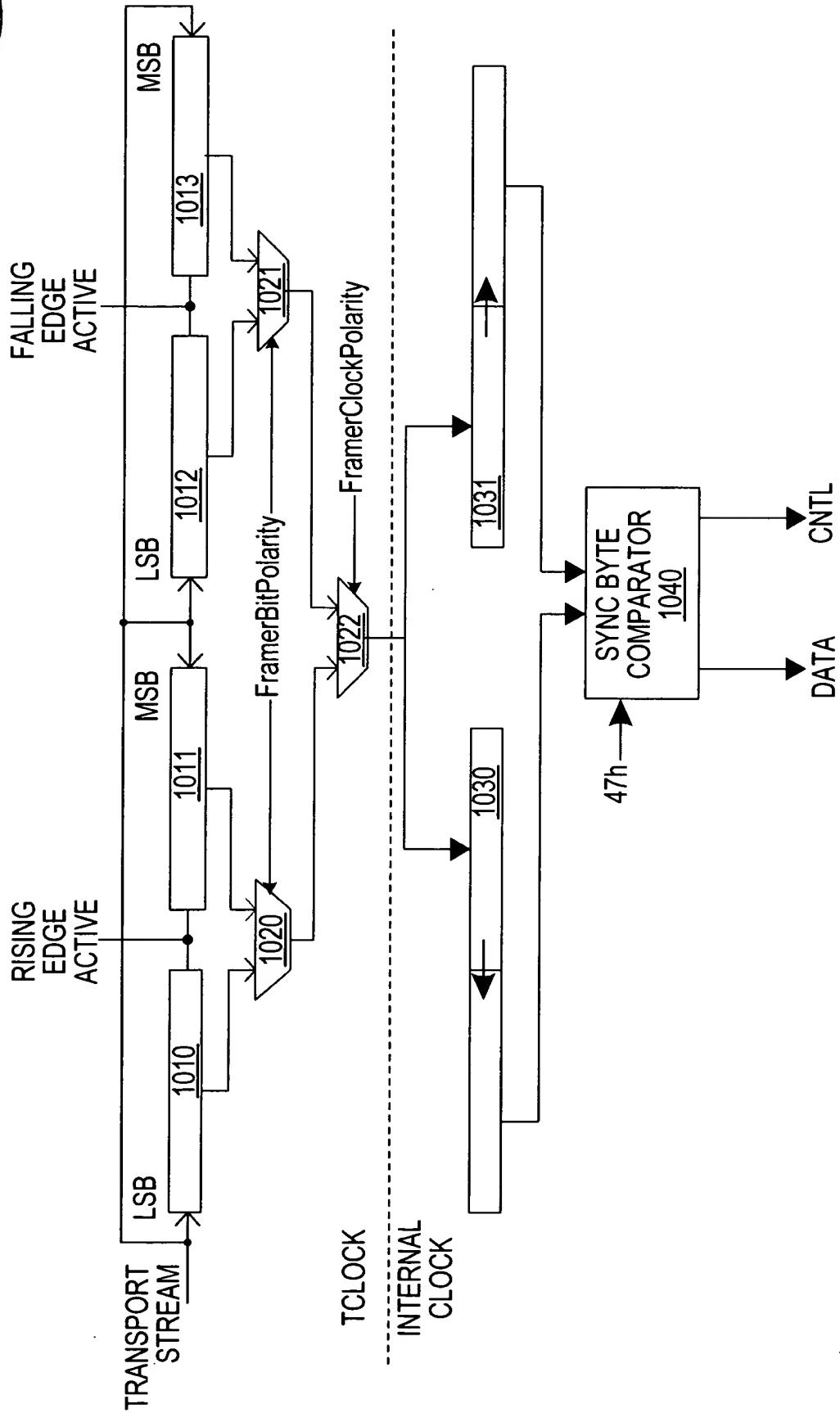
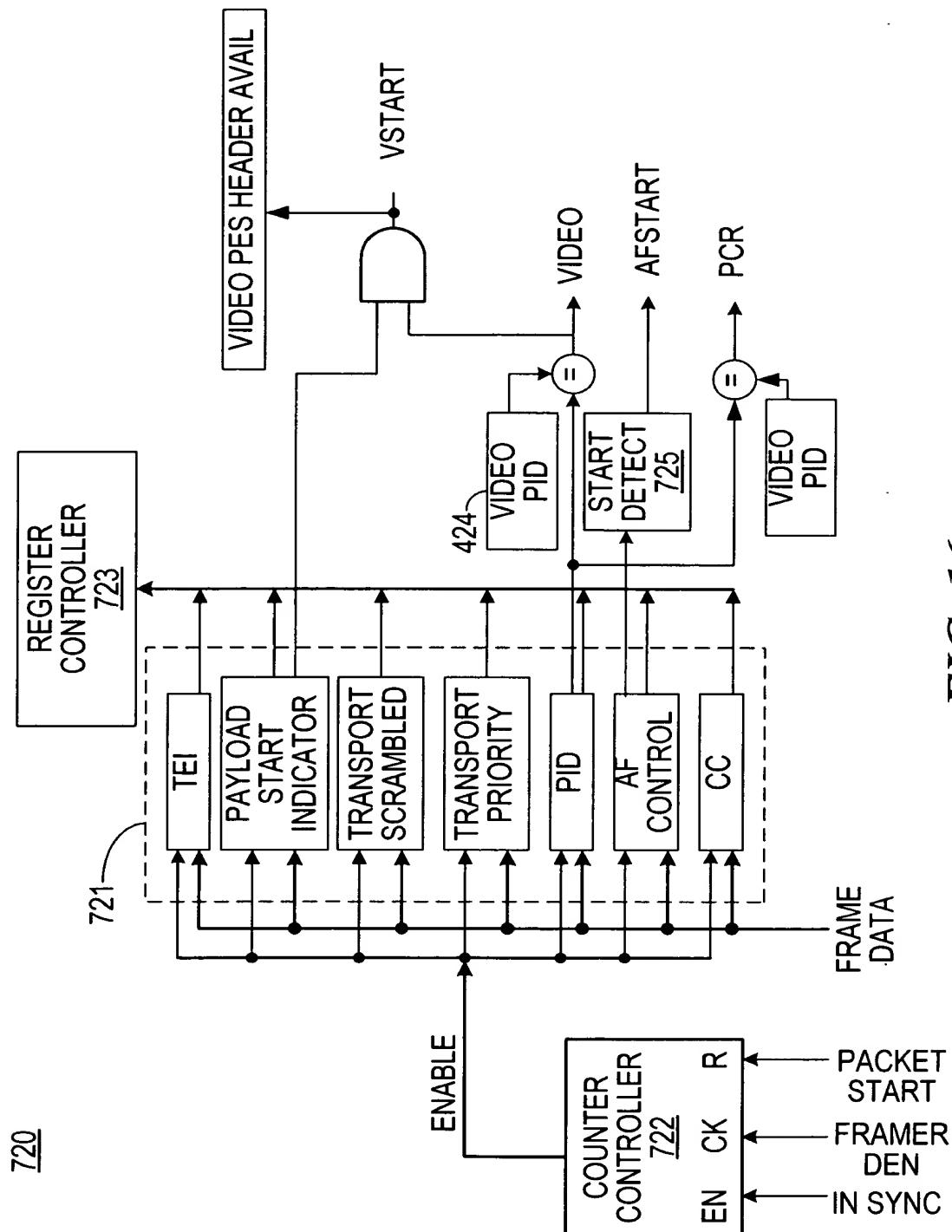


FIG. 15

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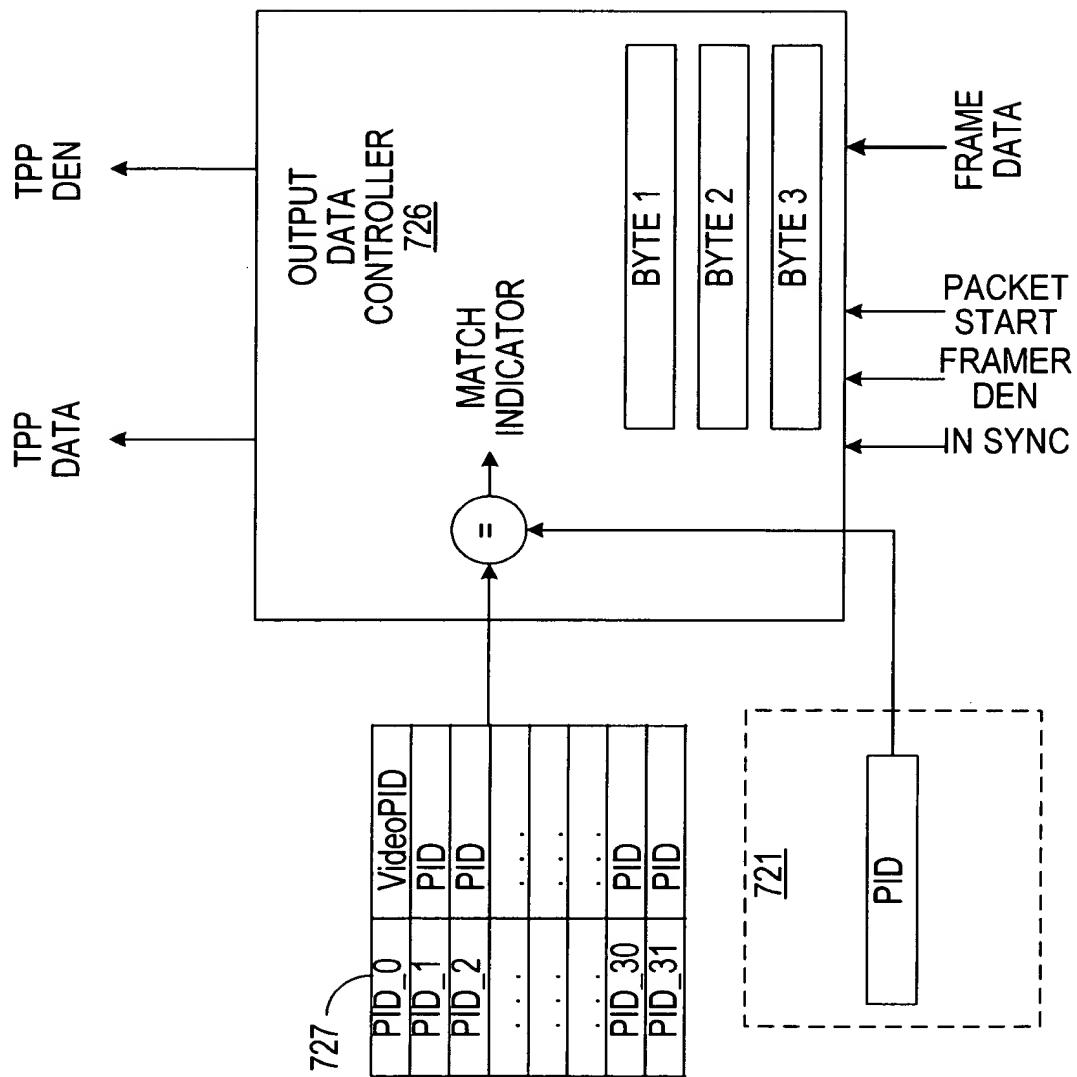


FIG. 17

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Video Control Registers					
Field Name	Bits	Len	Default	Type	Description
VideoPid	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the video component stream to filter on. Value of 4095 is reserved one (it means a NULL transport packets).
EnableParsing	13	[1]	0	R/W	If '1' enables parsing from the next transport packet.
StartFromPUSICCommand	14	[1]	0	R/W	'0' enables PES parsing immediately. '1' enables PES parsing a transport packet from new PES packet. After that, this bit auto-returns to 0.
ProcessStreamID	15	[1]	0	R/W	If '1' enables parsing on specific stream_id field.
StreamID	16-23	[8]	0xE0	R/W	stream_id of the ES stream to filter on in the PESP.

FIG. 18

Transport Demultiplexer Registers						
Field Name	Bits	Len	Default	Type	Description	
PID_yz,	$0 \leq yz \leq 30$	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the component stream to filter on. Value of 0x1FFF is reserved (it means a NULL transport packets).
EnableParsing	13	[1]	0	R/W	If set to '1' extraction of defined PID yz is enabled.	
BufferIndex	14-17	[4]	0	R/W	Specifies 1 of 16 destination buffers in the sys. mem.	

FIG. 19

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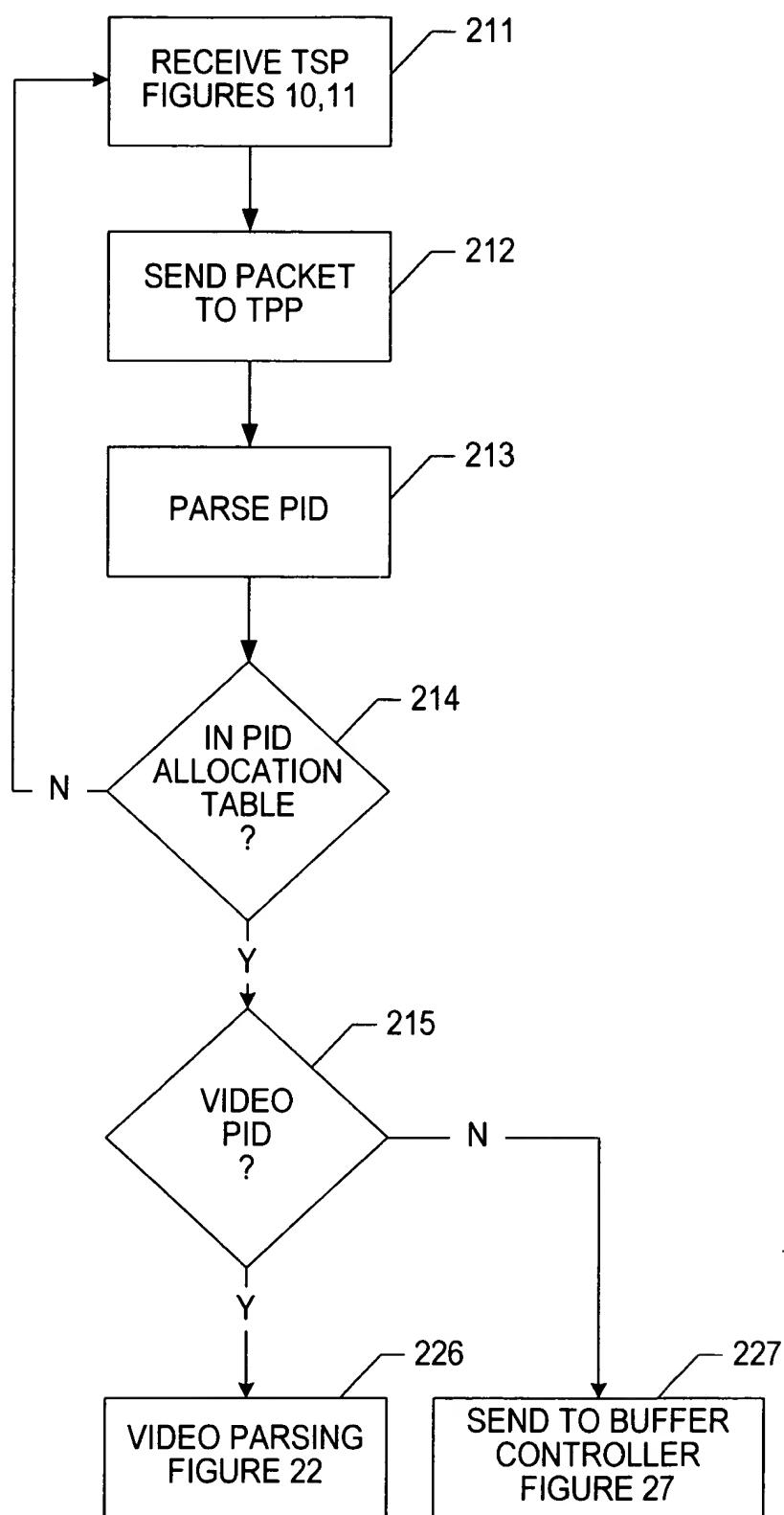


FIG. 20

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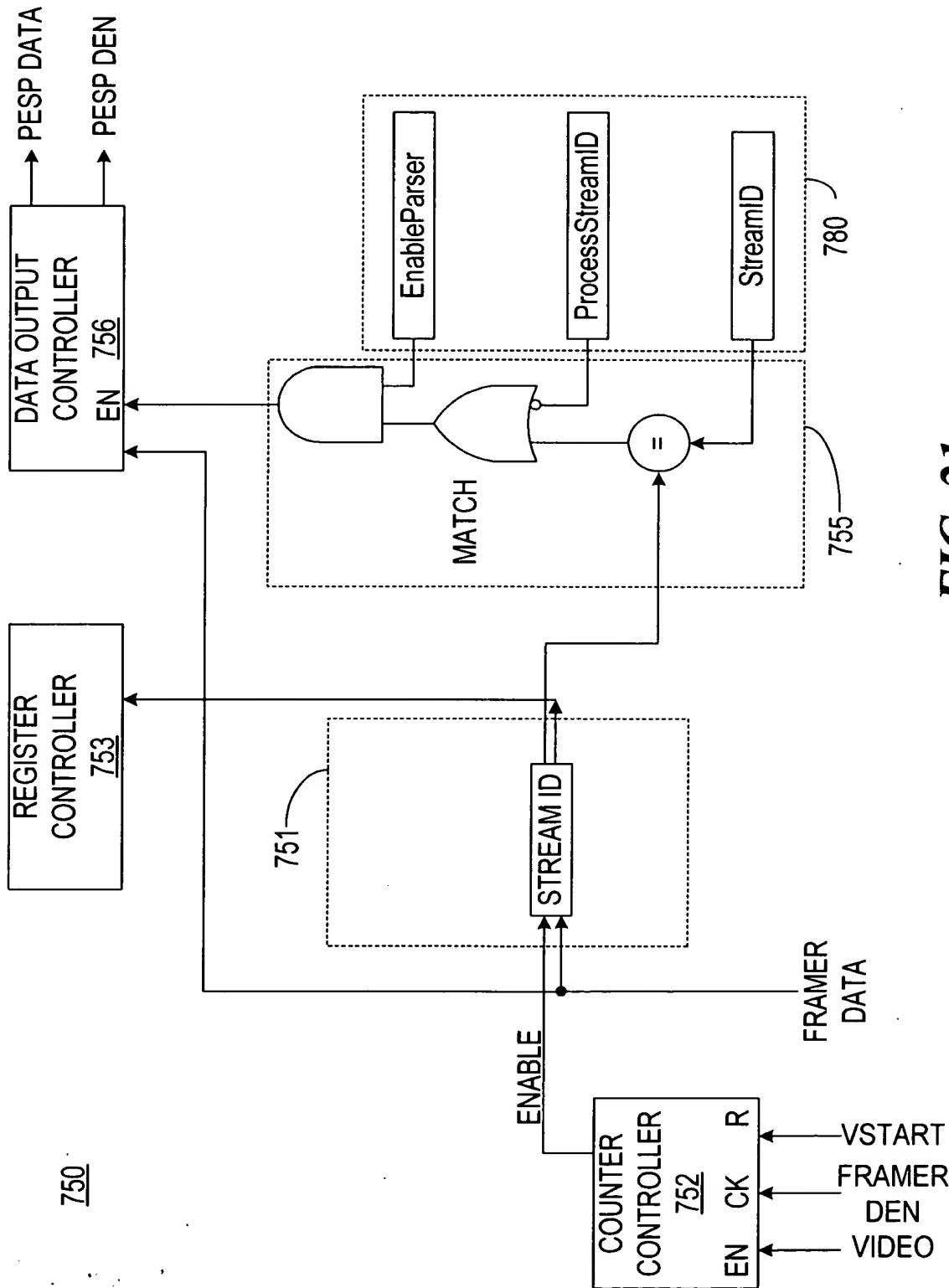


FIG. 21

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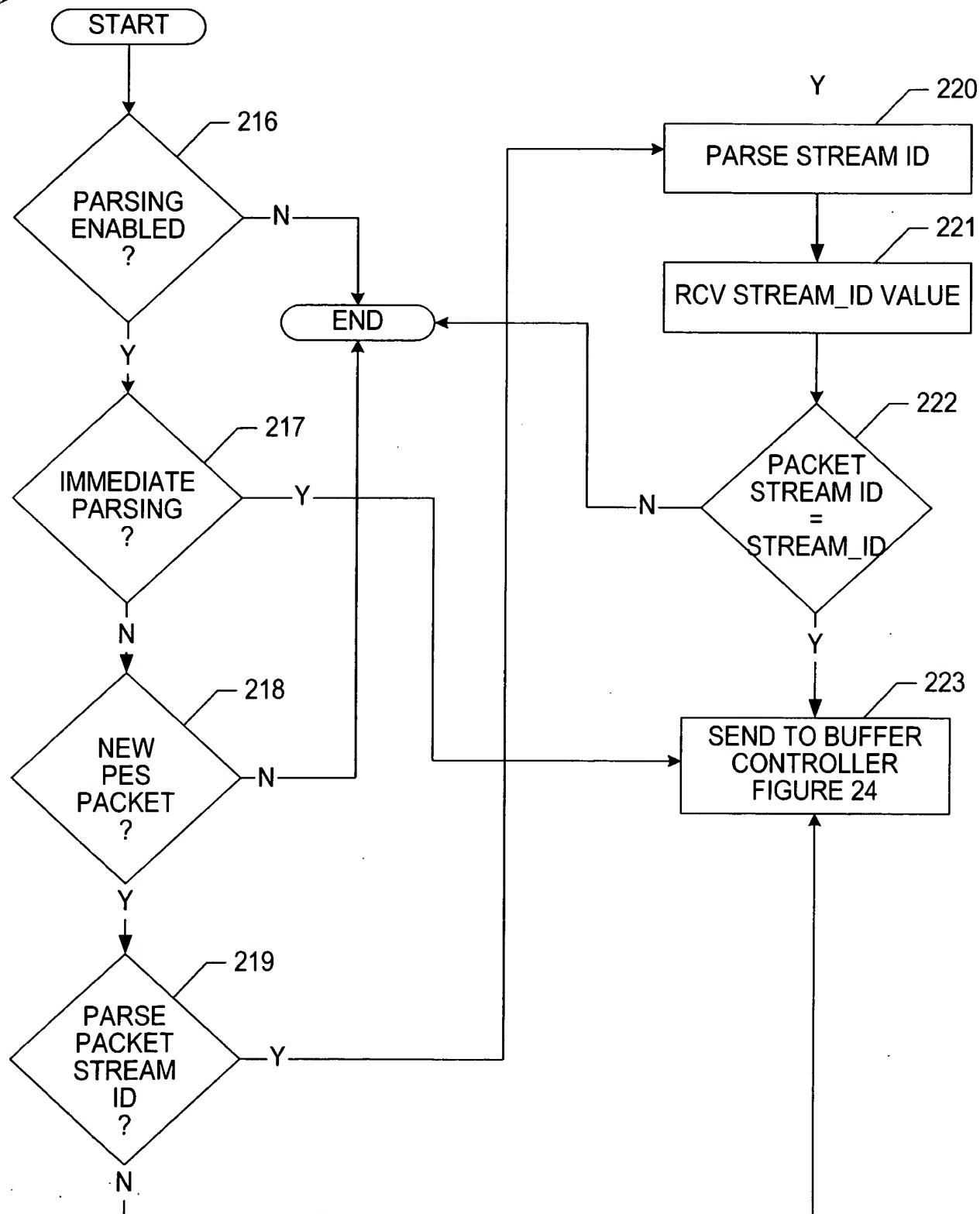


FIG. 22

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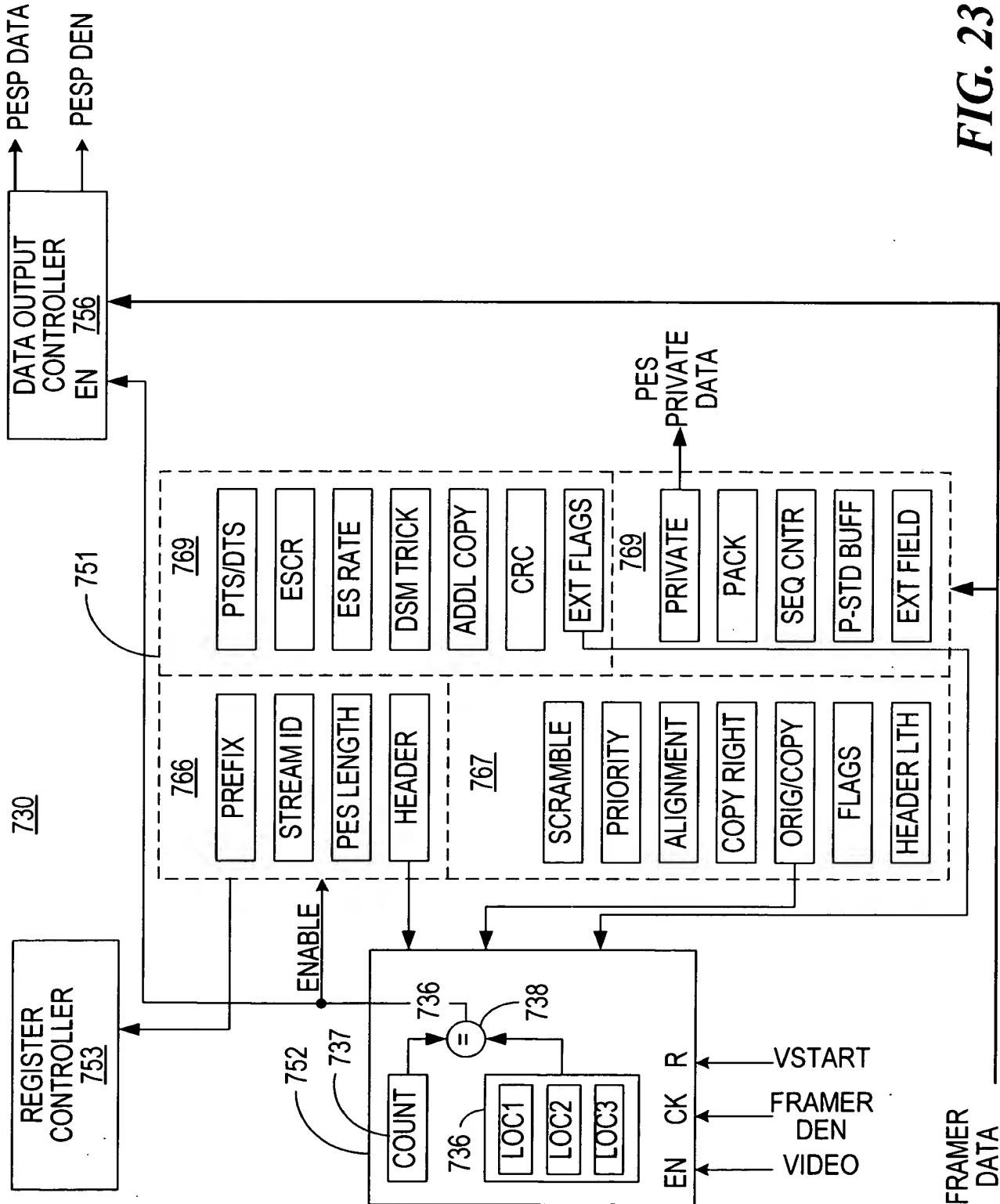
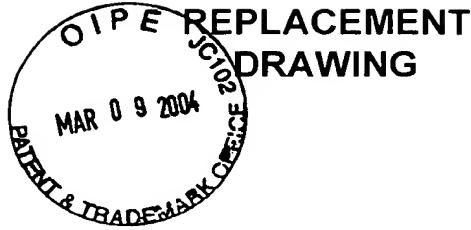


FIG. 23



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FIG. 24

Transport Demultiplexer Global Status Register					
Field Name	Bits	Len	Default	Type	Description
VideoPESHeaderAvailable	12	[1]	0	R/W	This bit is set to '1' when the new PES header of the video stream is received. WR ACC CLEAR.
VideoPESHeaderError	13	[1]	0	R/W	This bit is set to '1' after an error in the PES header is found. WR ACC CLEAR.
VideoPESDataAlignment	14	[1]	0	R/W	This bit is set to '1' when video PID has AF data alignment flag, indicating a possible start of I frame. WR ACC CLEAR.
VideoPESDSMTrickMode	15	[1]	0	R/W	Indicates that DSM data is found and extracted. WR ACC CLEAR.
VideoPESPriateData	16	[1]	0	R/W	This bit is set to '1' when video PID has 16 bytes of private data in the PES header. WR ACC CLEAR.
VideoPESCRCError	17	[1]	0	R/W	This bit is set to '1' if the video CRC of the PESP parser found a CRC mismatch. WR ACC CLEAR.

FIG. 25

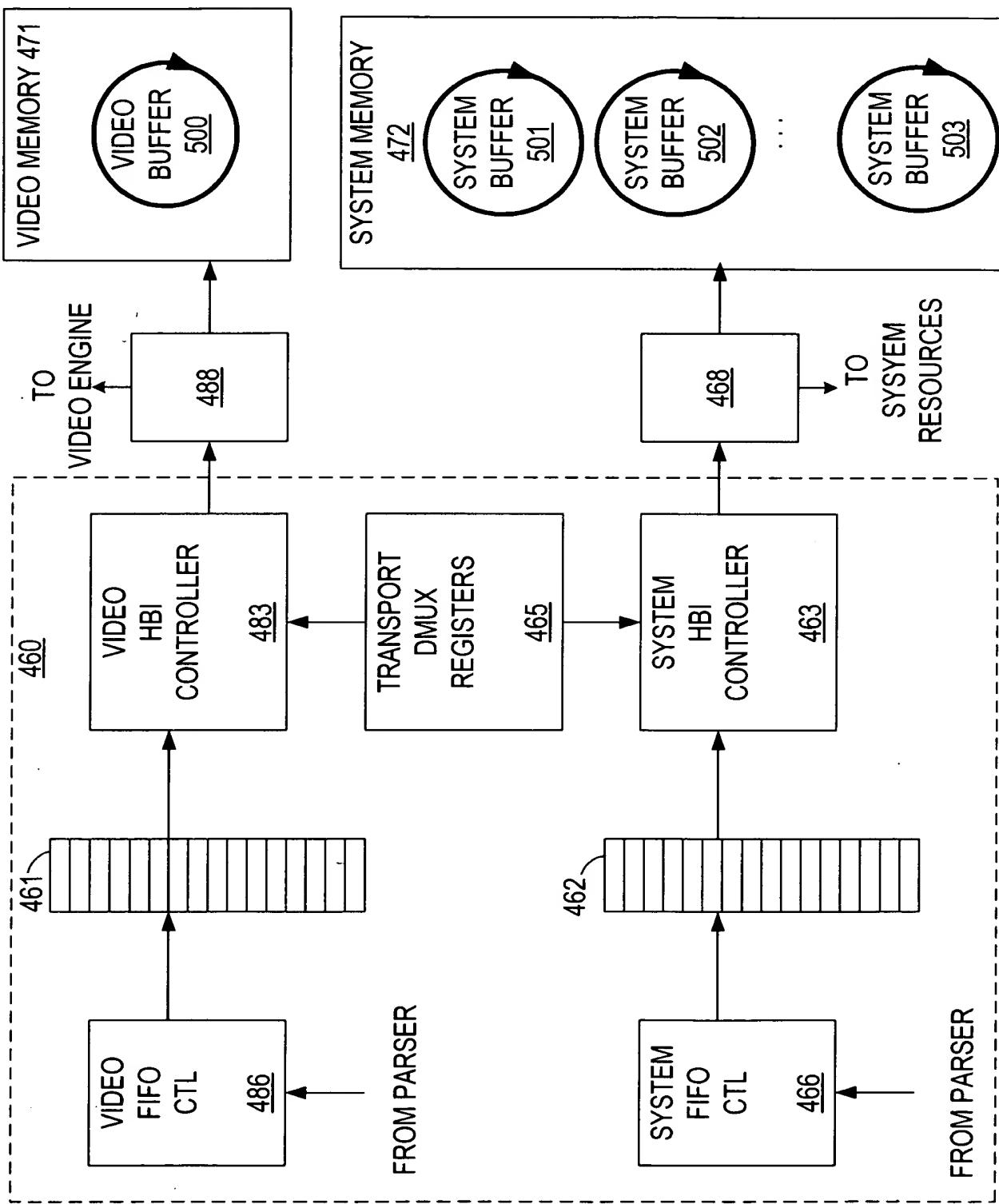
Transport Demultiplexer Interrupt Mask Register					
Field Name	Bits	Len	Default	Type	Description
EventInterruptMask	0-18	[19]	0	R/W	If set to '1' enables local sources Bit 12 – VideoPESHeaderAvailable Bit 13 – VideoPESHeaderError Bit 14 – VideoPESDataAlignment Bit 15 – VideoPESDSMTrickMode Bit 16 – VideoPESPrivateData Bit 17 – VideoPESCRCError Bit 18 – VideoPTSReceived Bit 19 – VideoESCRReceived

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FIG. 26



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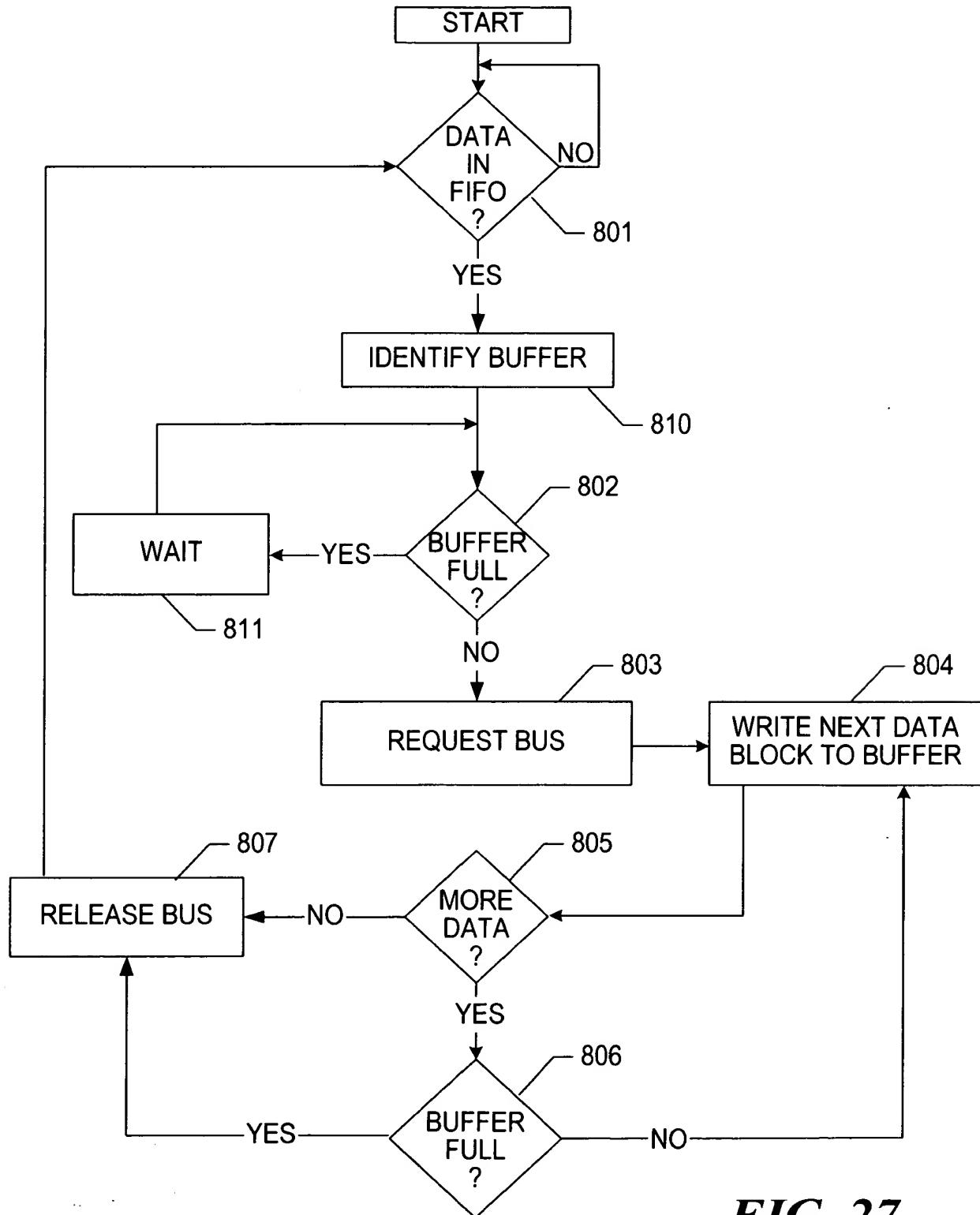


FIG. 27

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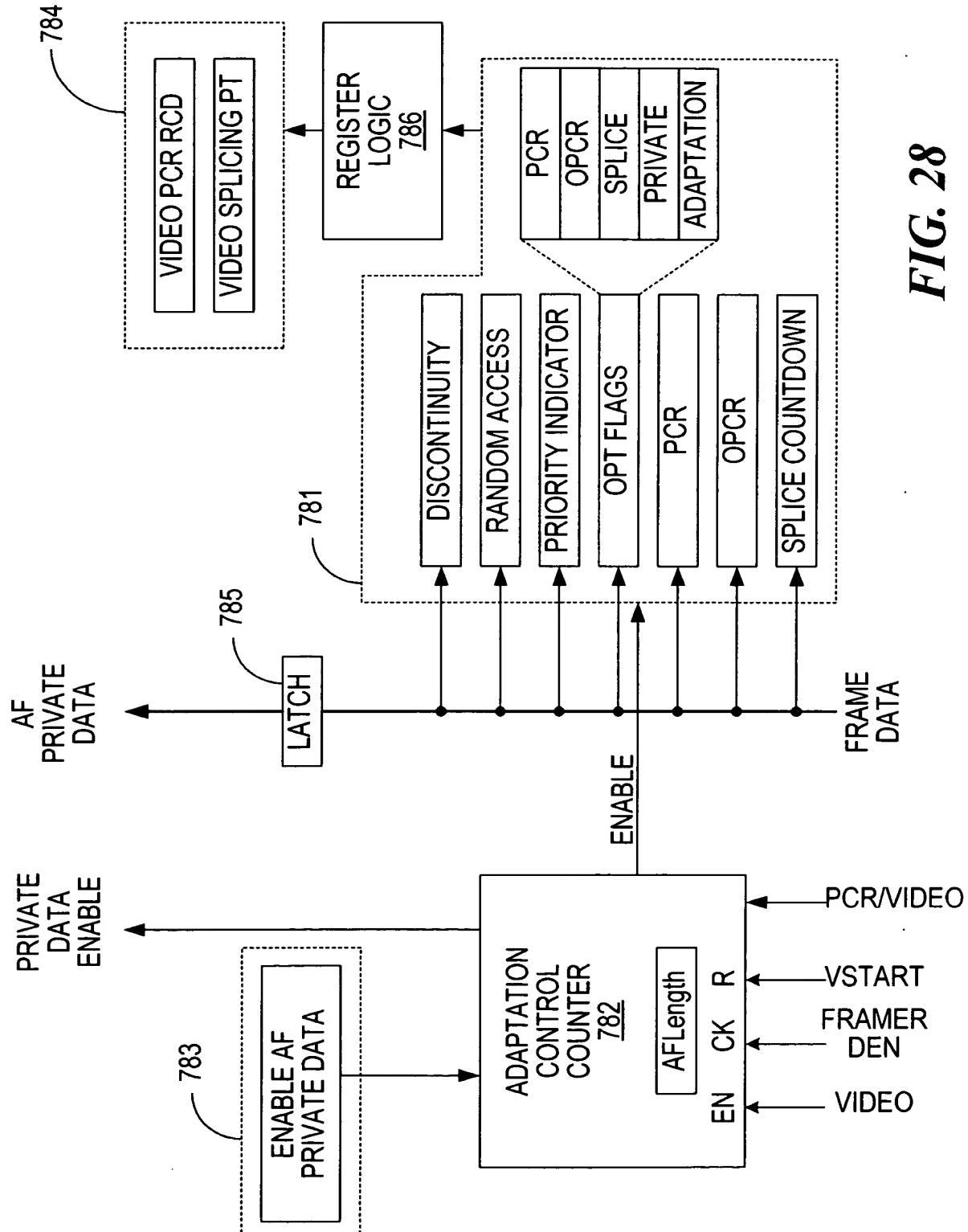


FIG. 28

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Transport Demultiplexer Global Status Register					
Field Name	Bits	Len	Default	Type	Description
VideoAFCrReceived	[1]	0	R/W	This bit is set to '1' after arrival and extraction of PCR sample in the adaptation field. WR ACC CLEAR.	
VideoAFCrDiscontinuity	[1]	0	R/W	This bit is set to '1' when a <i>discontinuity_indicator</i> in the adaptation field of the PCR PID is asserted. WR ACC CLEAR.	
VideoAFDiscontinuityFlag	[1]	0	R/W	This bit is set to '1' after a <i>discontinuity_indicator_flag</i> has been asserted in the AF of video TP, indicating a discontinuity on continuity_counter. WR ACC CLEAR.	
VideoAFRandomAccess	[1]	0	R/W	This bit is set to '1' when video PID has <i>random_access_flag</i> asserted in the AF, indicating a start of the elementary stream. WR ACC CLEAR.	
VideoAFSplicingFlag	[1]	0	R/W	This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, indicating approaching of the splicing point. WR ACC CLEAR.	
VideoAFSplicingPoint	[1]	0	R/W	This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, after splicing point occurred (<i>splice_countdown</i> =0). WR ACC CLEAR.	
VideoAFAccessData	[1]	0	R/W	This bit is set to '1' when video has AF private data. WR ACC CLEAR.	
AFSpliceCountdown	[8]	0x00	R/W	Current splice countdown value from adaptation field of A/V packets. Modified on the fly by AF content	

FIG. 29

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Transport Demultiplexer Interrupt Mask Register					
Field Name	Bits	Len	Default	Type	Description
EventInterruptMask	0-18	[9]	0	R/W	If set to '1' enables local sources Bit 5 – VideoAFPcrReceived Bit 6 – VideoAFPcrDiscontinuity Bit 7 – VideoAFDDiscontinuityFlag Bit 8 – VideoAFRandomAccessFlag Bit 9 – VideoAFSplicingFlag Bit 10 – VideoAFSplicingPoint Bit 11 – VideoAFPrivateData

FIG. 30

Transport Demultiplexer Global Control Register					
Field Name	Bits	Len	Default	Type	Description
EnableAFPrivateData	[1]	0		R/W	If '1' enables parsing and routing of AF private data
AFPrivateDataBufferIndex	[4]	0		R/W	Specifies 1 of 15 destination buffers in the system memory
PCRIndex	[1]	0		R/W	
EnableAutoSplicing	[1]	0		R/W	

FIG. 31

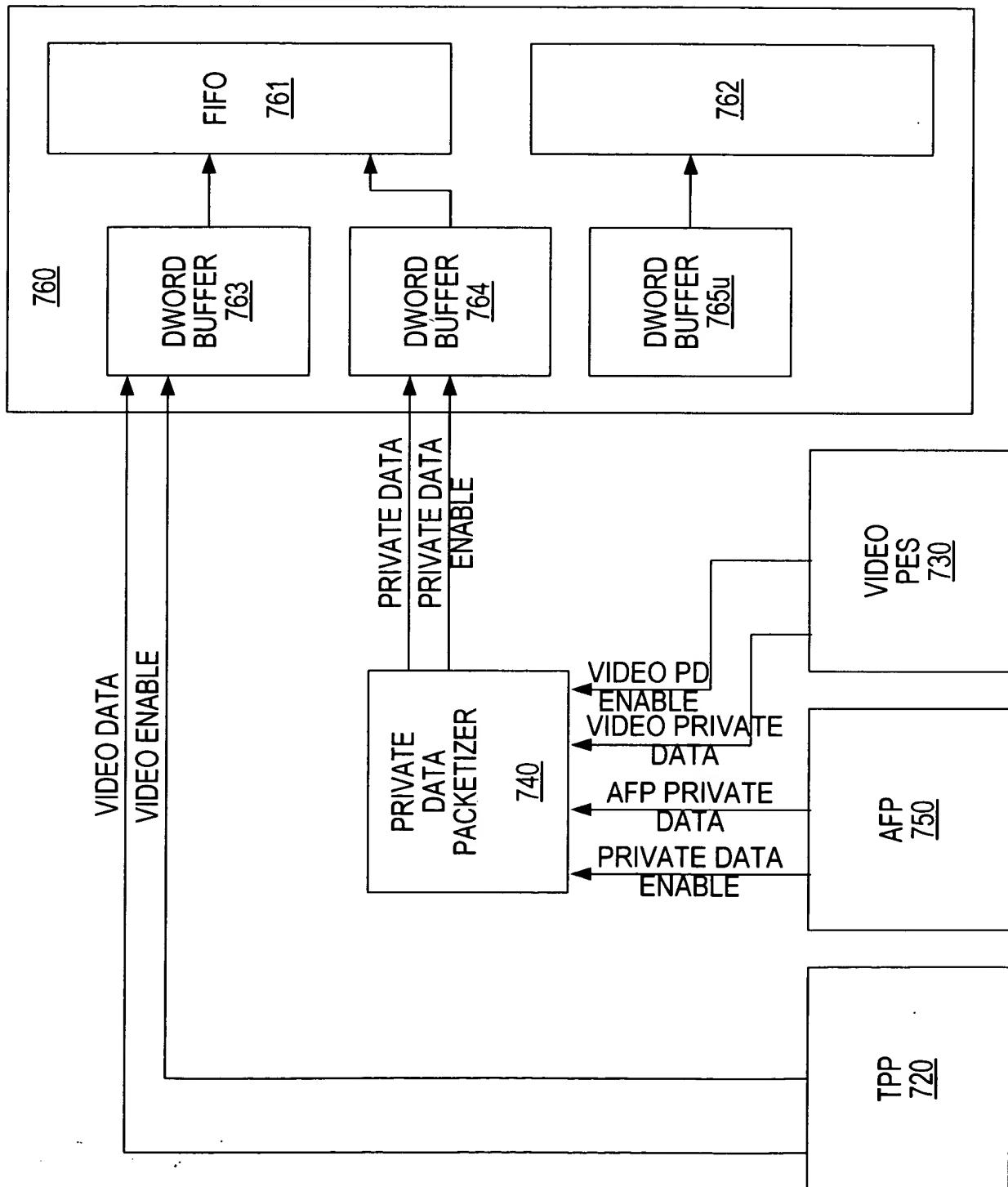
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FIG. 32



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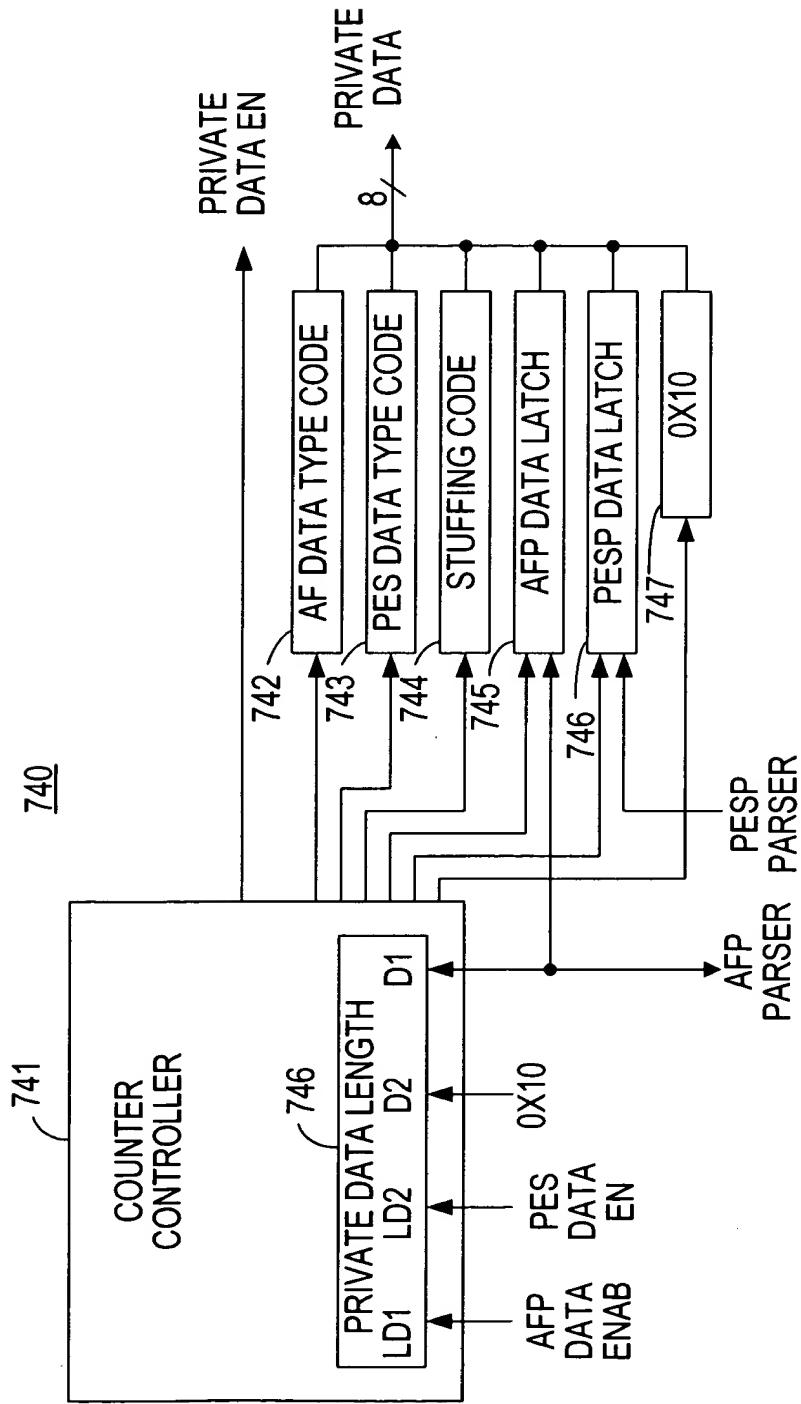
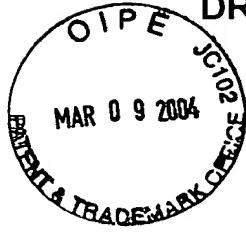


FIG. 33

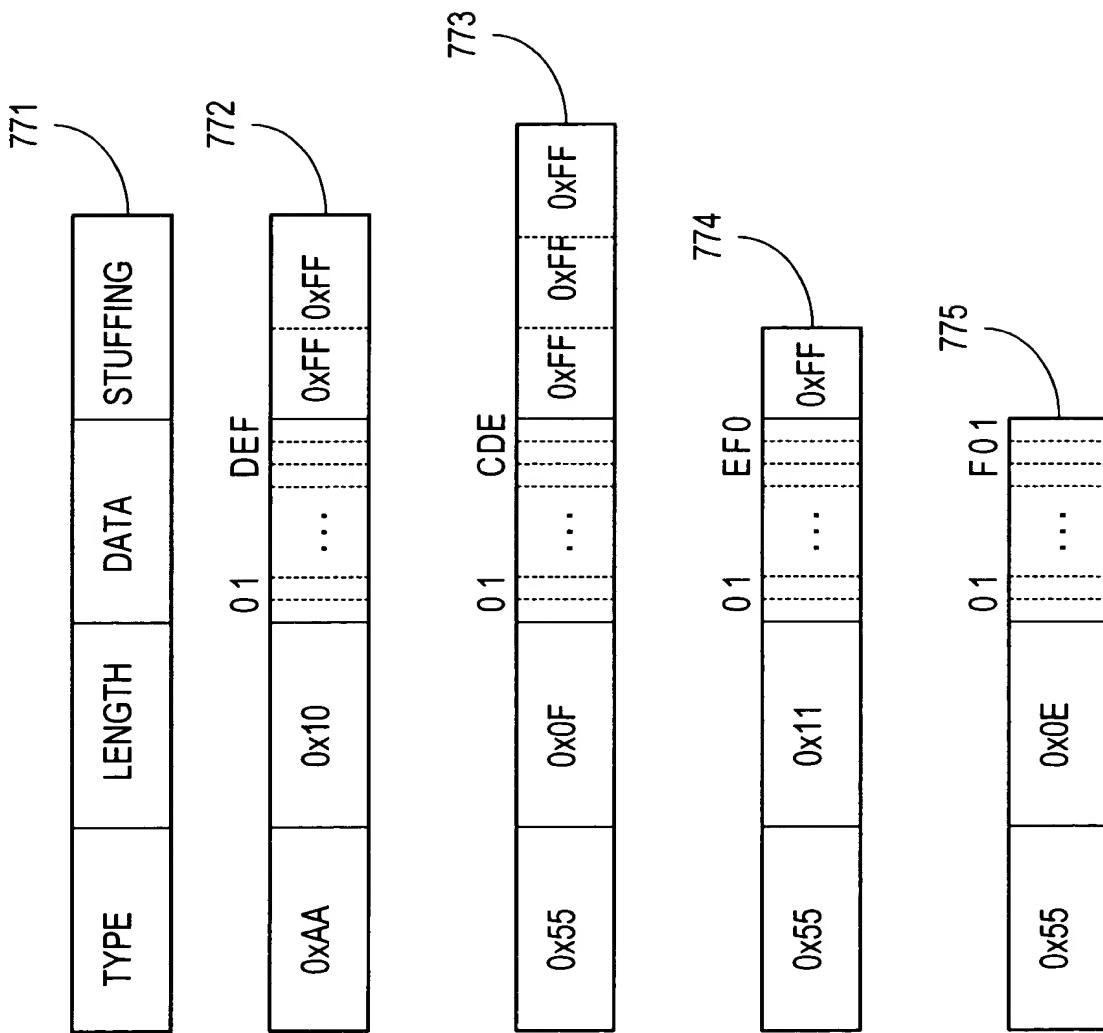
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FIG. 34



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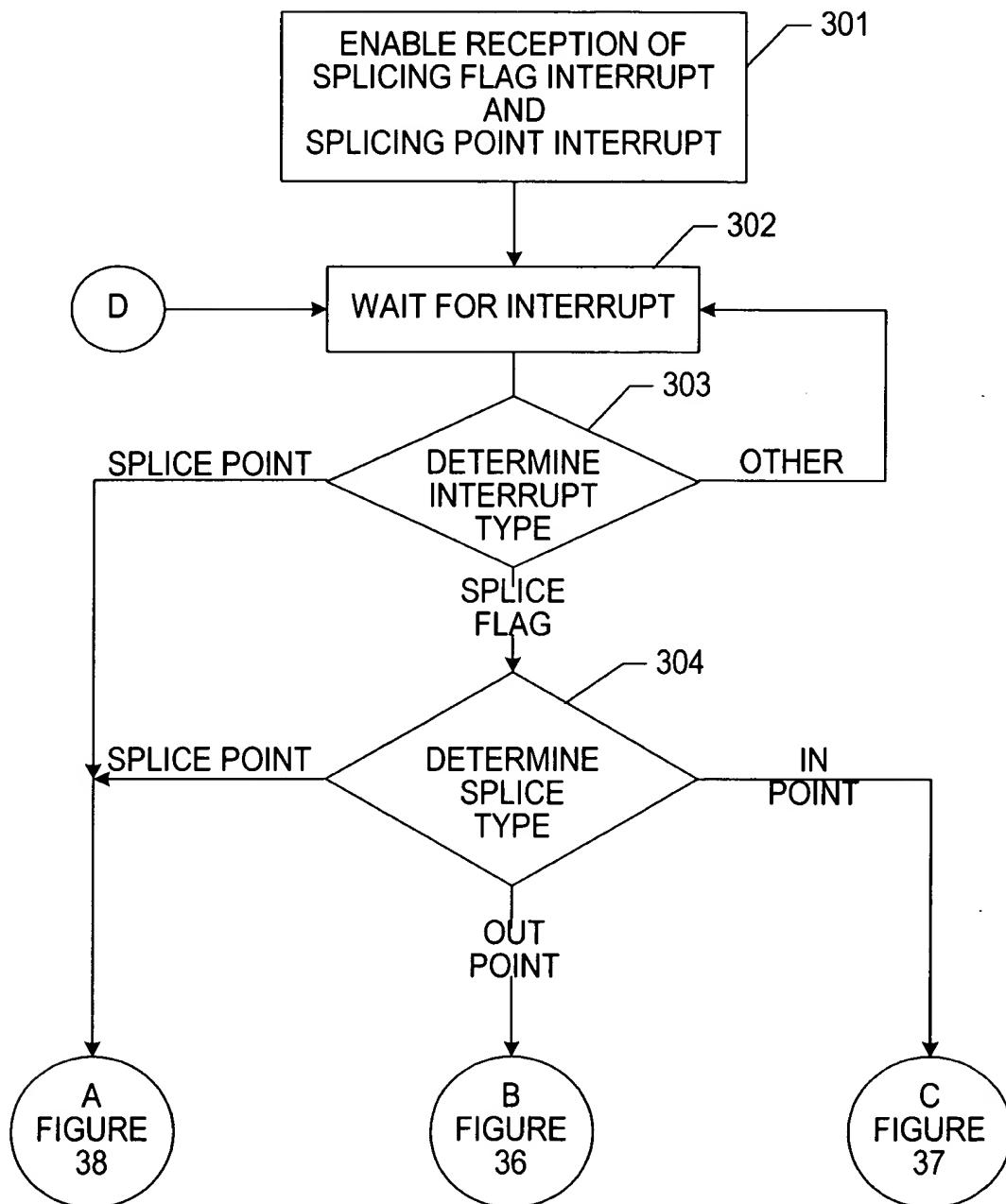
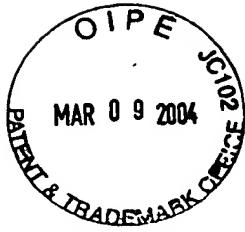


FIG. 35

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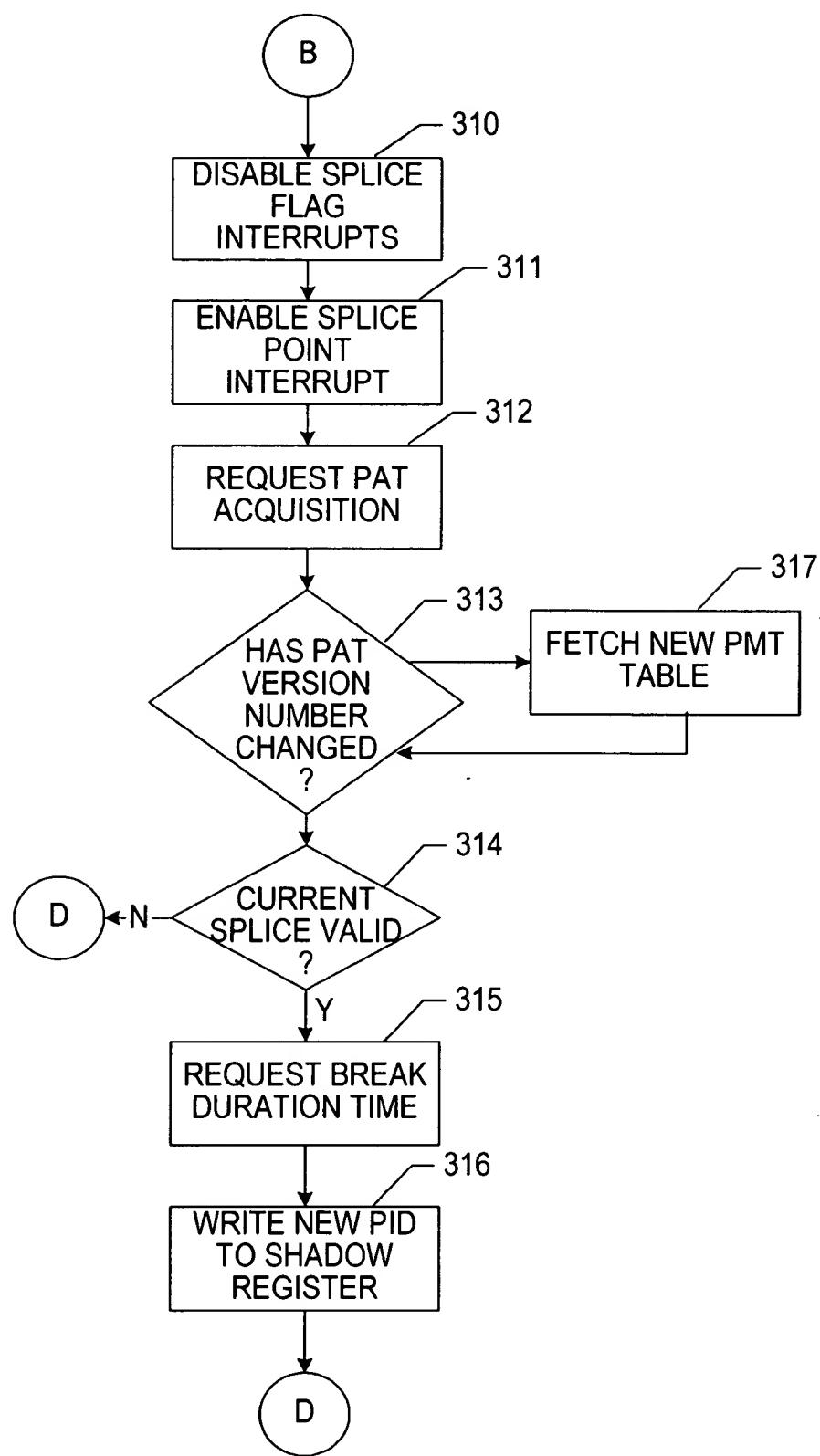


FIG. 36

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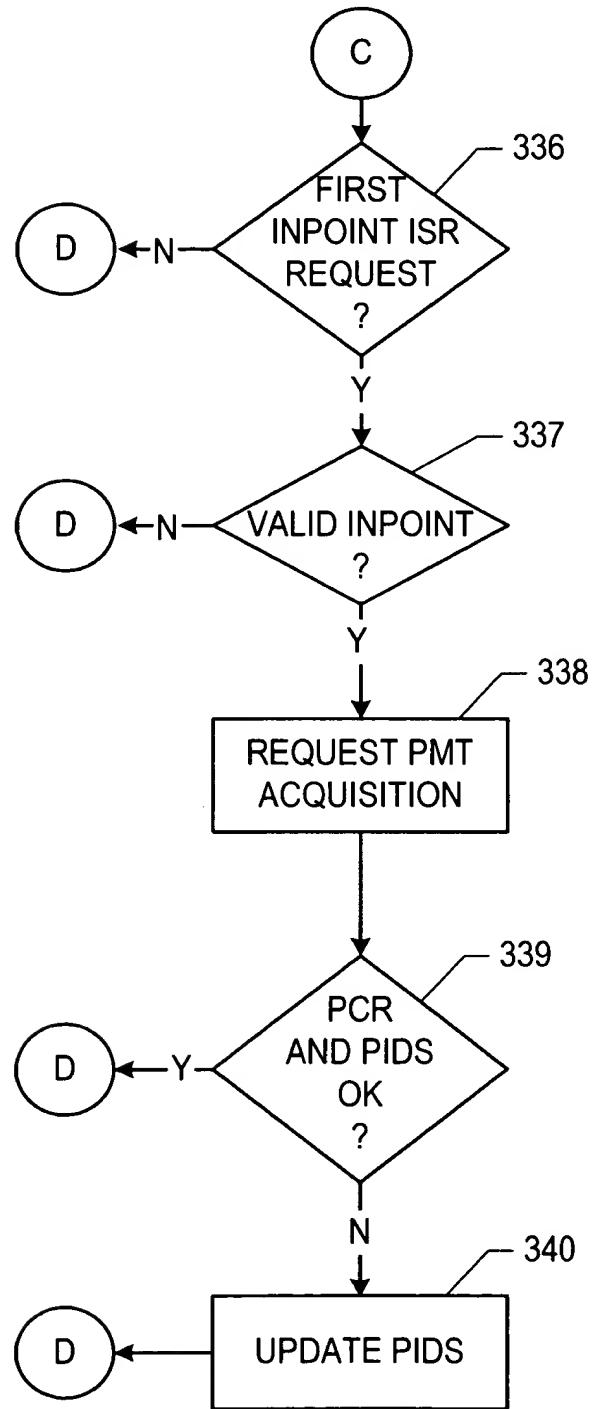


FIG. 37

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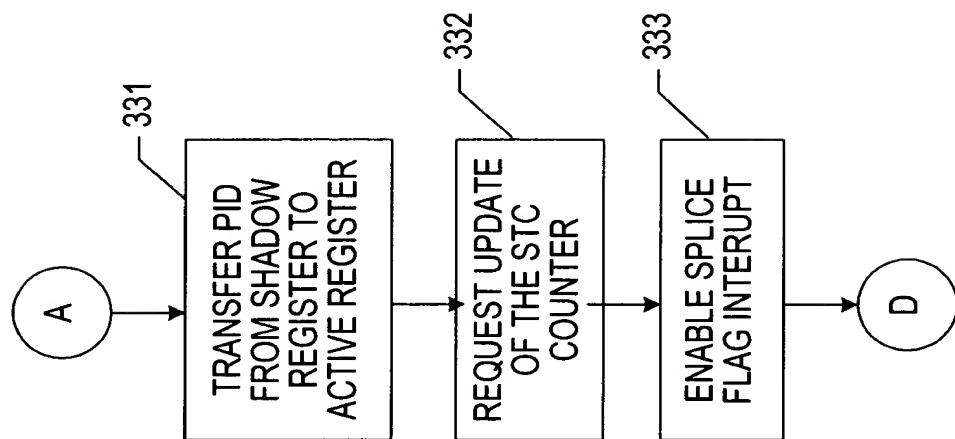


FIG. 38

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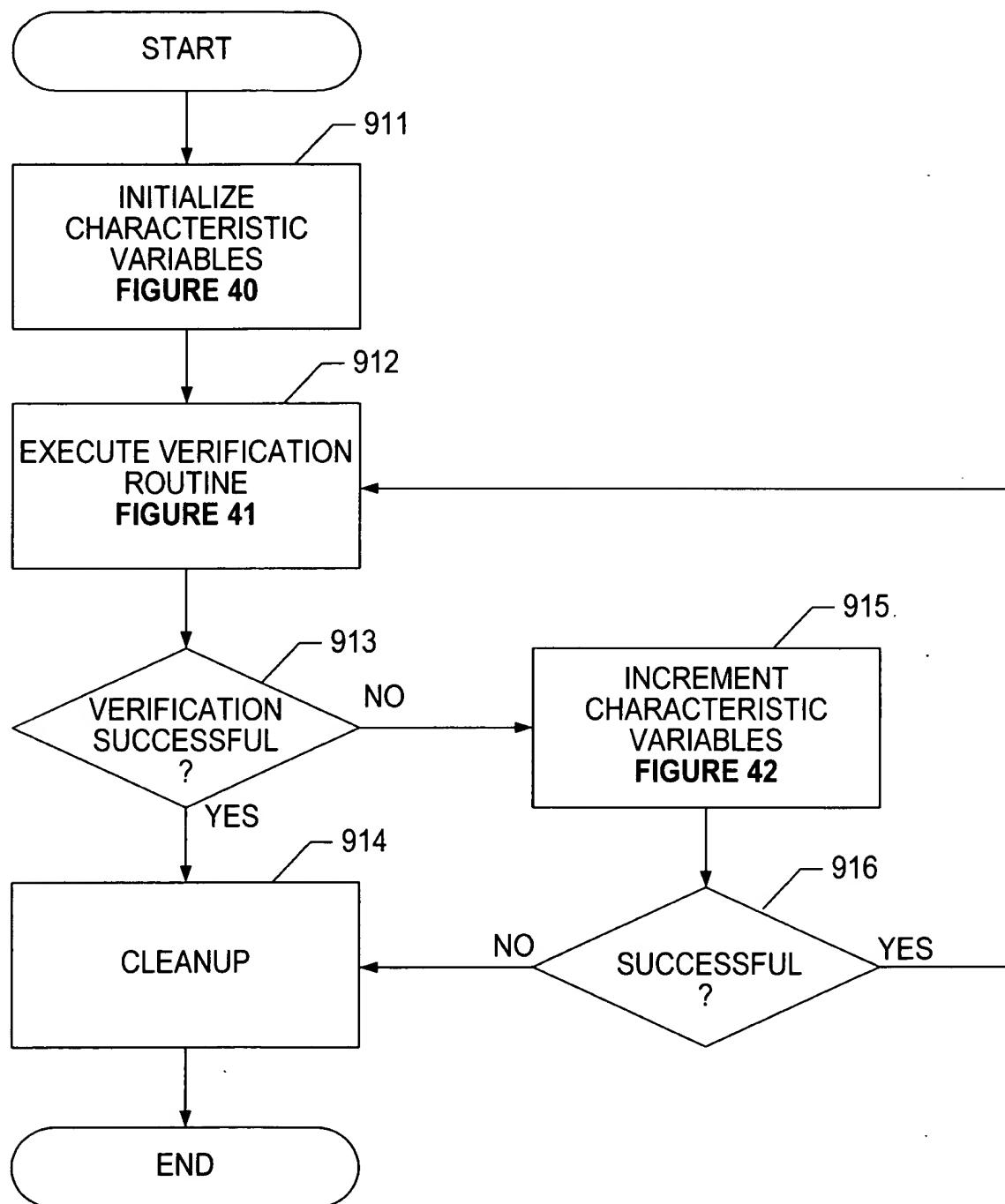


FIG. 39

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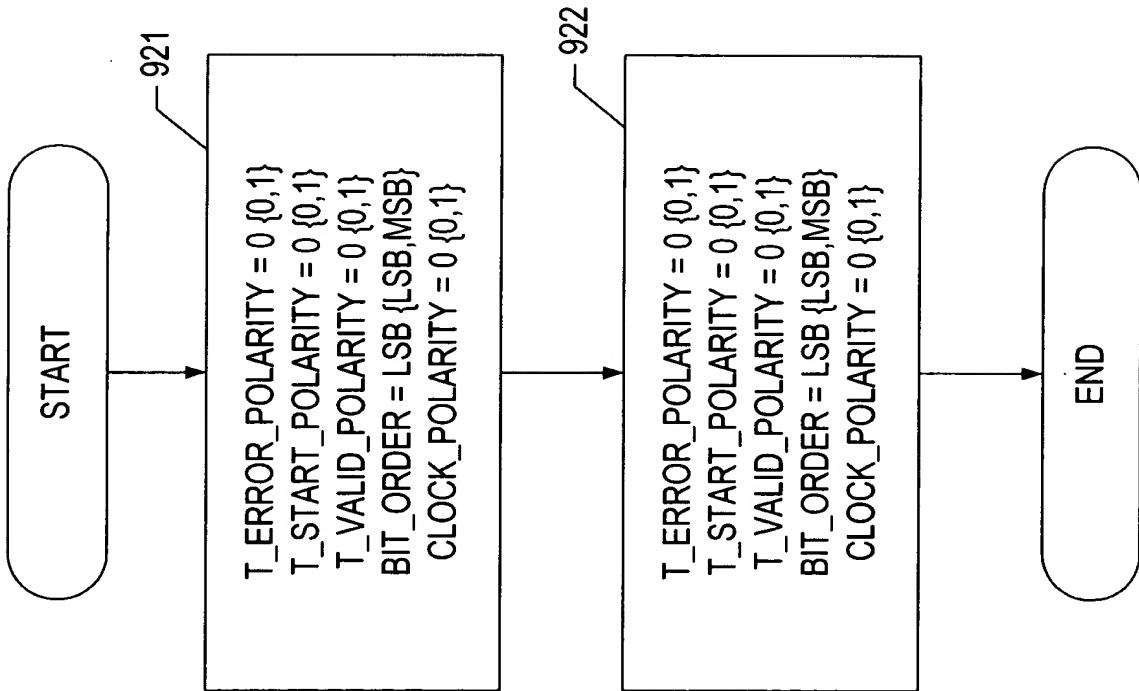


FIG. 40

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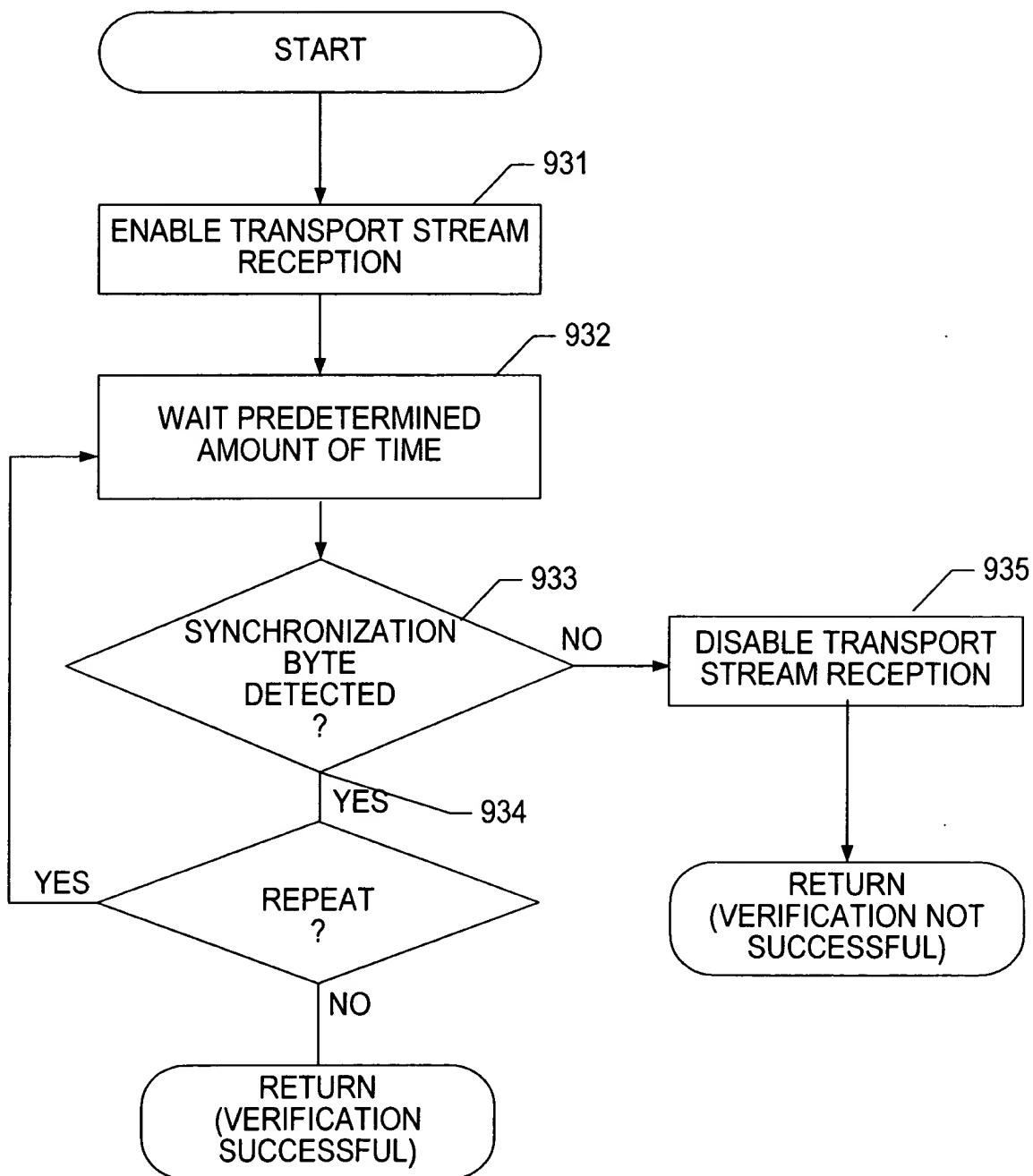


FIG. 41

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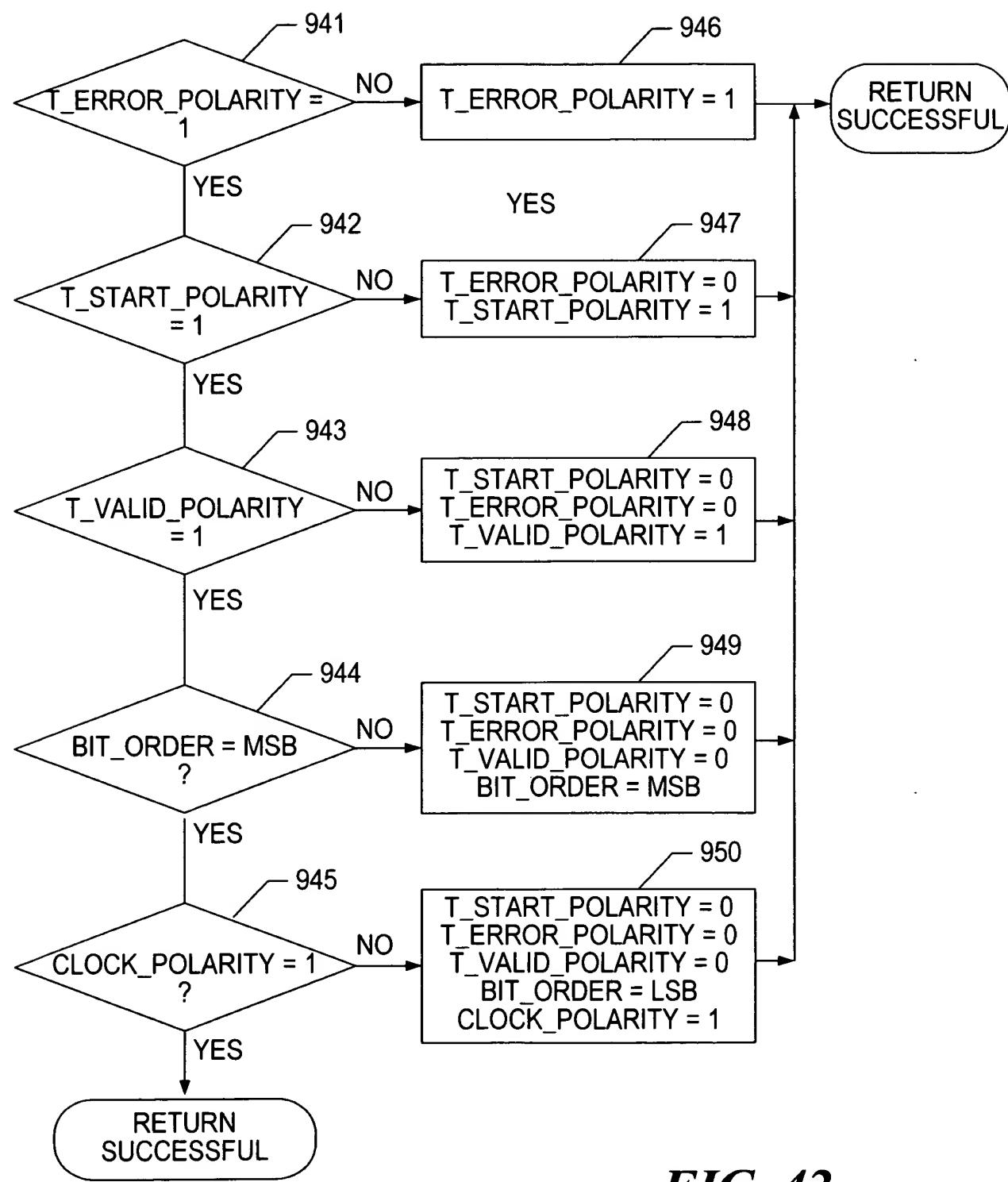


FIG. 42

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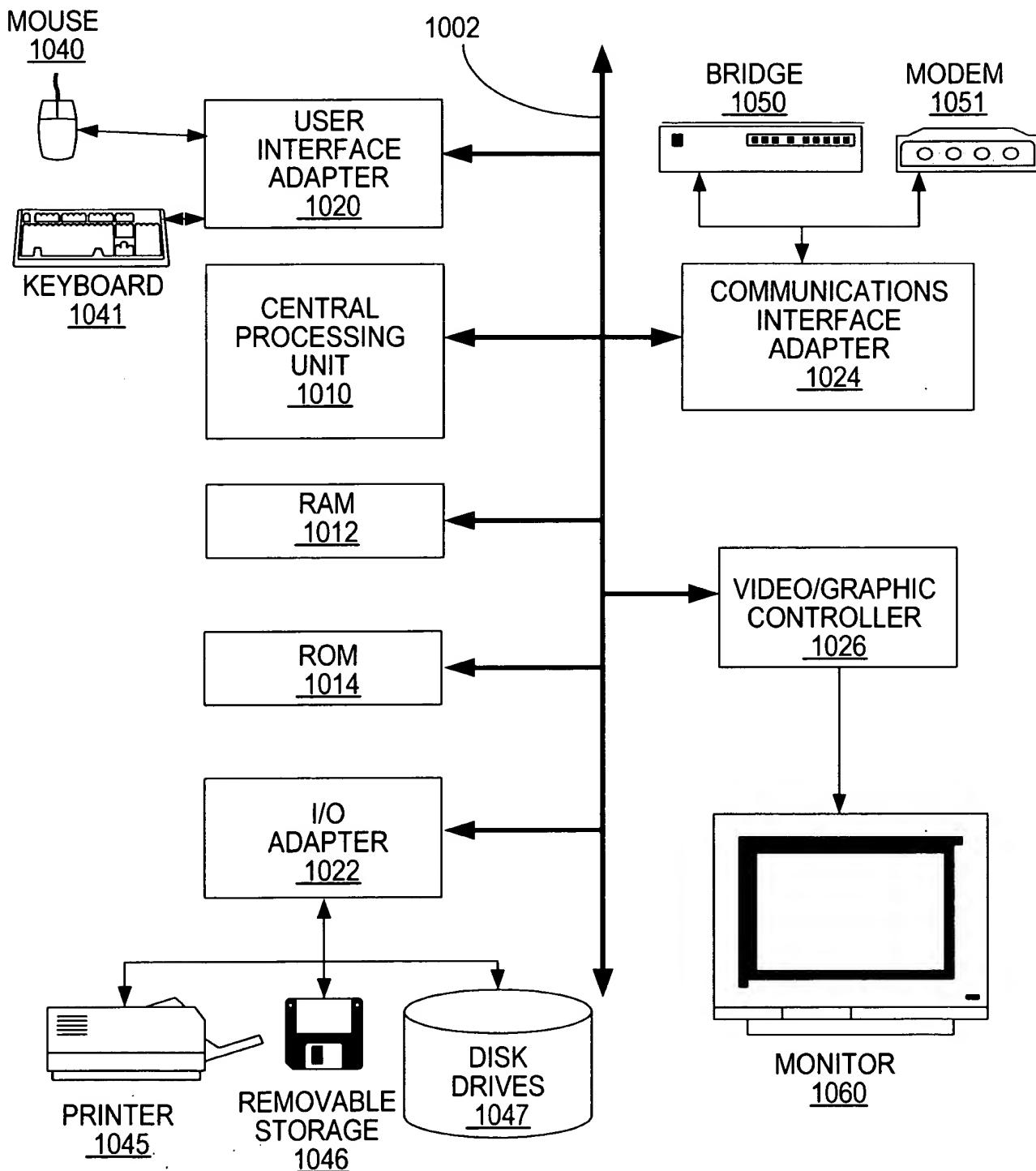


FIG. 43